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# NANOTUBES AND NANOWIRES

## Editor Peter John Burke

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## NANOTUBES AND NANOWIRES

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#### PREFACE

The field of nanotubes and nanowires is evolving at a rapid pace, with many potential applications in electronics, optics, and sensors, to name a few. In this special issue, several groups summarize some of these potential applications, although the list is by no means extensive. Rather, it is meant to serve as a flavor of and snapshot of the current state of the art in the field of nanowires and nanotubes. There is an ample mix of experimental, theoretical, and visionary material in this book to give the reader an indication of where the field is now, and where it is going.

Two chapters on the electrostatics and quantum properties of 1d FETs provide a snapshot of the understanding of device physics. One of the chapters focuses on a particular materials system (ZnO) for nanowire technology. Three chapters point to some of the potential applications, including sensors, memory, and high frequency electronics and systems.

While research continues at a rapid pace in academia and industry, the reader will get a good idea of the potential and current state of the art of the field, and will be in a better position to judge for themselves if and when the technology will find commercial applications.

Peter Burke Guest Editor Irvine, California This page intentionally left blank

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#### Nanostructured ZnO: Building Blocks for Nanoscale Devices

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ZnO is attracting intensive attention for its versatile applications in transparent electronics, UV emitter, piezoelectric devices, chemical sensor and spin electronics. As one of the direct wide band gap semiconductors, it has advantages over GaN due to its larger exciton binding energy, better lattice match on heteroepitaxial growth and availability of single crystal substrate. Large effort has been invested in the growth of nanostructured ZnO to explore its potentials for nanoscale device applications. ZnO nanobelts, nanowires, nanorings, and nanohelixes demonstrate the diversity of ZnO nanostructures family. This review presents recent research on ZnO nanostructures. Issues of synthesis methods, optical, electrical, gas sensing and magnetic properties are summarized. These progresses constitute the basis for developing future applications in nanoscale electronics, optoelectronics, chemical sensor and spintronics.

*Keywords*: wide band gap semiconductor; nanostructures; transparent electronics; UV emission; chemical sensor; spintronics

#### **1. Introduction**

Zinc oxide (ZnO) is one of the most important functional oxide semiconductors because of its unique properties and potential applications in manifold fields, such as transparent electronics, ultraviolet (UV) light emitter, surface acoustic wave (SAW) devices and spin electronics. Invisible thin film transistors (TFTs) using ZnO as an active channel achieve much higher field effect mobility (7 cm<sup>2</sup>/V·s) than amorphous silicon TFTs (0.5 cm<sup>2</sup>/V·s) [1-3]. ZnO has been proposed to be a more promising UV emitting phosphor than GaN because of its large exciton binding energy (60 meV), larger than the thermal energy at room temperature. This lowers the UV lasing threshold and yields higher UV emitting efficiency at room temperature [4]. Excitonic emissions have been observed from the photoluminescence spectra of ZnO nanorods [5]. Large scale vertically aligned ZnO nanorods have been synthesized, demonstrating the potential of fabricating nano-optoelectronics arrays [6]. SAW filters using ZnO films have already been used for video and radio frequency circuits. Piezoelectric ZnO thin film has been fabricated into ultrasonic transducer arrays operating at 100 MHz [7]. Holes mediated ferromagnetic ordering in bulk ZnO by introducing manganese (Mn) as dopant has been predicted theoretically [8] and reported recently [9]. Vanadium doped n-type ZnO films also demonstrate a Currie temperature above room temperature [10]. Due to these remarkable physical properties and the motivation of the device miniaturization trend, large efforts have been focused on nanoscale ZnO materials to fabricate high density, high speed, low power devices. An assortment of ZnO nanostructures, such as nanorods, nanowires, and nanorings, have been successfully grown via a variety of methods including chemical vapor deposition, thermal evaporation, and electrodeposition [11-14]. These nanostructures have been subjected to electrical transport [15,16], UV emission [4,17], gas sensing [18], and ferromagnetic doping [9,19,20] studies, and considerable progresses have been achieved. In this paper, recent research achievements on ZnO nanostructures are reviewed, summarizing studies on their synthesis methods, structural, mechanical, electrical, sensing, optical, and magnetic properties.

#### 2. Synthesis and characterization of ZnO nanostructures

ZnO nanostructures are usually obtained via a vapor transport process. Depending on the synthesis condition variations in temperature, catalyst, and composition of source materials, a wide range of nanostructures has been obtained. Using a vapor-solid process, complex ZnO nanostructures such as nanohelixes, nanorings and nanobelts were synthesized by Kong et al. [21] (Fig. 1a). In this process, ZnO powder was decomposed into  $Zn^{2+}$  and  $O^{2-}$  at ~1400 °C then transported by Ar carrier gas to a low temperature zone (~400 °C), and nanostructures were formed on a collecting chip. In a similar vapor transport and condensation process reported by Ren et al. [22, 23], hierarchical ZnO nanostructures were grown by mixing ZnO, In<sub>2</sub>O<sub>3</sub> and graphite powder and heated up to 820-870 °C. A simplified method to achieve nanowires, nanoribbons and nanorods was reported by Yao et al. [13]: ZnO powder was mixed with graphite and heated to 1100 °C then cooled down, nanostructures were found to form on the wall of the furnace. These synthesis methods utilize the vapor-solid (VS) mechanism, in which ZnO nanostructures are formed by condensing directly from vapor phase. Although diverse nanostructures can be obtained, this method provides less control on the geometry of ZnO nanostructures. Controlled growth of ZnO nanowires has been achieved by using various nanoparticles or nanoclusters as catalysts, such as Au [24, 25], Cu [26], and Co [27]. In these cases, ZnO and carbon powder are usually used as source material and a vapor-liquid-solid (VLS) growth mechanism governs the synthesis. In the VLS mechanism, the catalyst nanoparticles become liquid droplet under reaction temperature. The reactant Zn vapor generated by carbon thermal reduction of ZnO powder is transported to the catalyst nano-droplets and form Zn-catalyst alloy. In the meantime, ZnO forms as a result of the reaction between Zn and CO/CO<sub>2</sub>. Upon suppersaturation, ZnO nanowires grow from the droplets. Recently we have found that this synthesis process can be further simplified by directly heating pure Zn powder in low concentration oxygen environment (2%) using Au nanoparticles as catalysts [28]. The as-synthesized nanowires show high quality and they grow along (0001) direction, as indicated in Figs. 1b & 1c. The advantage of using nanoparticles as catalysts lies in the better control of the nanostructure growth. Based on the VLS mechanism, the diameter of nanowire can be tuned by using different size nanoparticle catalysts. Yang et al. reported achievements of ZnO nanowires growth in controlling the position, orientation, diameter and density [4]. In their method, (110) plane sapphire was used as an epitaxial substrate to obtain vertically grown ZnO nanowires along the (001) direction (Fig. 1d). Besides using sapphire as epitaxy substrate, anodic alumina membranes (AAM) was utilized

as templates to obtain highly ordered ZnO nanowire arrays [14,15]. These well-controlled synthesis methods pave the way to the integration of ZnO nanostructures for future large scale device applications.

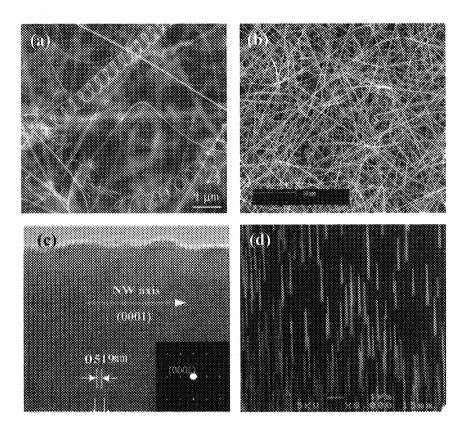


Fig. 1. (a) ZnO nanohelix structures grown via Vapor-Solid process. (reprint permission from ref. [21]) (b) ZnO nanowires grown via VLS process. (c) High resolution TEM image of a ZnO nanowire shows growth direction along (0001). (d) Vertical aligned ZnO nanowires array on sapphire substrate. (reprint permission from ref. [4])

#### 3. Mechanical properties of ZnO nanostructures

Understanding the fundamental physical properties is central to the rational design of functional devices. Investigation on individual ZnO nanostructures is critical to their applications in nanoelectronic devices and systems. Direct measurement of mechanical behavior of individual nanostructures is rather challenging since the traditional measurement method for bulk material does not apply. Based on an electric-field-induced resonant excitation, Bai [29] *et al.* characterized the bending modulus of ZnO nanobelts using transmission electron microscopy (TEM). In this method, a special TEM sample holder was

made to apply an oscillating electric field between a ZnO nanobelt and a fixed electrode. This electric field drove the vibration of the nanobelt, and resonant oscillation was achieved by tuning the driving frequency, as depicted in Fig. 2. Following the classical elasticity theory, bending modulus was calculated and shown in Table 1. ZnO nanobelt demonstrates to be a promising material for nanoresonator and nanocantilever. Its small size renders improved sensitivity compared with conventional cantilever fabricated by microtechnology. Hughes [30] *et al.* reported manipulation of ZnO nanobelt to the desired length and position. This could lead to the usage of nanobelt as highly sensitive atomic force microscopy probe.

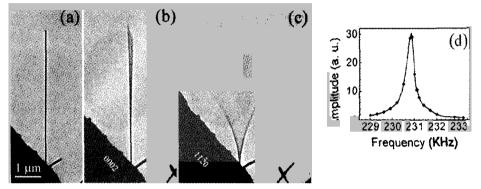


Fig. 2 TEM images of a ZnO nanobelt at (a) stationary (b) the first harmonic resonance in x (thickness) direction,  $v_x = 622$  KHz, (c) the first harmonic resonance in y (width) direction,  $v_y = 691$  KHz. (d) Resonance peak of a ZnO nanobelt. (reprint permission from ref. [29])

Table1. Bending modulus of ZnO nanobelts. Ex and Ey represents for the modulus along thickness and width direction. (reprint permission from ref. [29])

Nanobelt	L (µm) W (	Width W (nm)	(nm) T (nm)	Fundamental frequency (kHz)				Bending modulus (GPa)	
		(±1)		₩4T	r'x1	բյլ	$v_{y1}/v_{y1}$	Ex	E,
1	8.25	55	33	1.7	232	373	1.6	46.6±0.6	50.1±0.0
2	4.73	28	19	1.5	396	576	1.4	44.3±1.3	45.5±2.9
3	4.07	31	20	1.6	662	958	1.4	56.3±0.9	64.6±2.3
4	8.90	44	39	1.1	210	231	1.1	37.9±0.6	39.9±1.2

#### 4. Electrical properties

Electrical transport measurements have been performed on individual ZnO nanowires and nanorods [16, 31-33]. Fan [31] *et al.* configured single ZnO nanowires as field effect transistors using photolithography. Nanowires synthesized by CVD method were dispersed first in isopropanol alcohol to form nanowires suspension, then deposited onto  $SiO_2/Si$  substrate. Photolithography was used to define contact electrodes array. Degenerately doped Si substrate was used to serve as a back gate, and the neighboring electrodes contacting a nanowire function as source and drain. Due to native defects such as oxygen vacancies and

zinc interstitials, ZnO nanowires are reported to be *n*-type semiconductor. Figure 3a shows *I-V* characteristics under different back gate voltages. Well defined transfer characteristic is shown in Fig. 3b. Carrier concentration and mobility are derived from the transfer characteristic of the nanowire transistor to be  $\sim 10^7$  cm<sup>-1</sup> and  $\sim 17$  cm<sup>2</sup>/V·s, respectively. It is worth noting that the CVD grown ZnO nanostructures are usually single crystalline, rendering them superior electrical property than polycrystalline thin film. For example, an electron field effect mobility of 7 cm<sup>2</sup>/V·s is regarded quite high for ZnO thin film transistors [2]. However, single crystalline ZnO nanowires showed much higher mobility, as Chang *et al.* had reported an electron mobility of 80 cm<sup>2</sup>/V·s. This indicates that the ZnO nanostructures based device can achieve a faster operation speed than their thin film counterpart. Furthermore, using a uniquely designed synthesis setup, one can modify the carrier concentration and mobility of the nanowires (Fig. 3c), providing a way to tune the electrical property of ZnO nanowires [28].

The major impediment of ZnO for broad electronics and photonics applications rests with the difficulty of p-type doping. Several p-type doping efforts have been reported, with a Ga and N codoping method, low resistivity (0.5  $\Omega$ cm) p-type ZnO thin film was obtained [34]. Look et al. reported nitrogen-doped p-type ZnO obtained by molecular beam epitaxy with a hole mobility of 2 cm<sup>2</sup>/V s [35]. Kim et al. reported phosphorus-doped p-type ZnO with a thermal activation process [36]. Successful p-type doping for ZnO nanostructures will greatly enhance their potential applications for nanoscale electronics and optoelectronics. P-type and n-type ZnO nanowires can serve as p-n junction diodes and light emitting diodes (LED). And field effect transistors (FET) fabricated from them can constitute complementary logic circuits. Combined with their optical cavity effect, electrically driven nanowire laser can be potentially implemented. An attempt to make intramolecular p-n junction on ZnO nanowires was performed by Liu et al [15]. In this case, anodic aluminum membrane was used as a porous template with pore size around 40 nm. A two step vapor transport growth was applied and boron was introduced as the p-type dopant in the first step. Consequently, the I-V characteristics demonstrated rectifying behavior due to the intramolecular p-n junction in the nanowire.

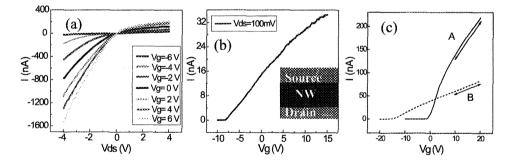


Fig. 3 (a) *I-V* curves of a ZnO nanowire FET from Vg = -6V to 6V; (b) Transfer characteristic of a ZnO nanowire FET (inset); (c) Transfer characteristics of two nanowires with different carrier concentration and carrier mobility. Nanowire A has a mobility of 80 cm<sup>2</sup>/V·s and carrier concentration ~ $10^6$  cm<sup>-1</sup>; and nanowire B has a mobility of 22 cm<sup>2</sup>/V·s and carrier concentration ~ $10^7$  cm<sup>-1</sup>.

#### 5. Electron field emission from vertical aligned ZnO nanostrucures

Quasi-one-dimensional (Q1D) nanomaterial with sharp tip is a natural candidate for electron field emission. In fact, field emission from vertical aligned ZnO nanoneedles and nanowires have been investigated by many groups [27, 37-39]. Tseng [37] *et al.* grew needle-like ZnO nanowires on Ga-doped ZnO film at 550°C, the as-grown nanowires showed well-aligned vertical structure as shown in Fig. 4a. These nanowires were subject to field emission measurement, the turn-on field was found to be ~18 V/µm at a current density of 0.01 µA/cm<sup>2</sup>, and the emission current could reach 0.1 mA/cm<sup>2</sup> at 24 V/µm, as shown in Fig. 4b. Lee [27] *et al.* reported better results for ZnO nanowires synthesized at low temperature. They obtained a turn-on field of 6 V/µm at a current density of 0.1 µA/cm<sup>2</sup>, and the emission current reached 1 mA/cm<sup>2</sup> at 11 V/µm, which could provide sufficient brightness to flat panel display.

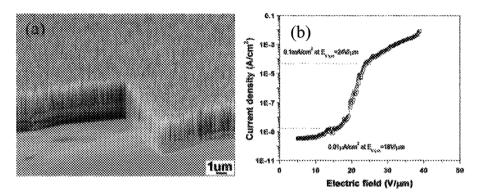


Fig. 4 (a) Vertically aligned ZnO nanowires on Ga-doped ZnO film; (b) Emission current-voltage characteristics of ZnO nanowires. (reprint permission from ref. [37])

#### 6. Chemical sensing and hydrogen storage with ZnO Nanostructures

Oxygen vacancies on metal-oxide surfaces are electrically and chemically active. These vacancies function as *n*-type donors, often significantly increase the conductivity of oxide. Upon adsorption of charge accepting analytes at the vacancy sites, such as NO<sub>2</sub> and O<sub>2</sub>, electrons will be depleted from the conduction band, leading to a reduced conductivity of the *n*-type oxide. On the other hand, molecules that react with surface oxygen, such as CO and H<sub>2</sub>, would react with surface adsorbed oxygen and remove it, leading to an increase in conductivity. Most metal-oxide gas sensors operate based on this principle. As one of the major materials for solid state gas sensor, bulk and thin films of ZnO have been proposed for CO [40], NH<sub>3</sub> [41], alcohol [42] and H<sub>2</sub> [43] sensing under elevated temperature (~400 °C). From the aspect of sensing performance, quasi-one-dimensional (Q1D) ZnO, such as nanowires and nanorods, is expected to be superior than its thin film counterpart. When their diameter is small and comparable to the Debye length, chemisorption induced surface states virtually affect the electronic structure of the entire channel, thus render Q1D ZnO higher sensitivity than thin film. In addition, ZnO nanowires and nanorods can be configured as

either two terminal sensing devices or as FETs in which an external electric field can be utilized to tune the sensing property. Recently, Wan [18] et al. fabricated ZnO nanowires gas sensor using microelectromechanical system technology. Massive nanowires were placed between Pt interdigitating electrodes. Under an operation temperature of 300 °C, the resistance of nanowires significantly decreases upon exposure to ethanol (Fig. 5a). Electrical transport studies show that  $O_2$  ambient has considerable effect on the ZnO nanowires [16, 31]. Fan et al. discussed the relationship between oxygen pressure and ZnO nanowire FET performance [31]. It is shown that ZnO nanowires have fairly good sensitivity to  $O_2$  (Fig. 5b). In addition, it is observed that the sensitivity is a function of back gate potential, *i.e.*, above gate threshold voltage of FET, sensitivity increases with decreasing gate voltage (Fig. 5b inset). This implies that the gate voltage can be used to adjust the sensitivity range. In addition, the large surface-to-volume ratio of nanowires not only results in their enhanced gas sensing performance, but also facilitates potential hydrogen storage property. Wan [44] et al. investigated hydrogen storage characteristics under room temperature. The highest storage of 0.83 wt% was achieved at a pressure of 3.03 MPa. In this work, it was suggested that hydrogen storage was due to not only surface adsorption but also the incorporation of  $H_2$  into the crystal interstitial sites.

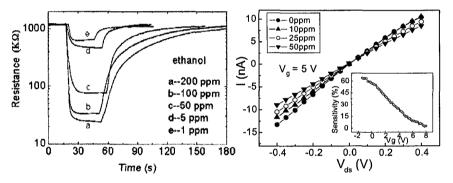


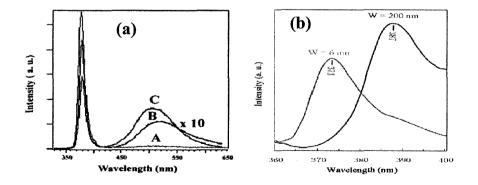
Fig. 5 (a) Response of ZnO nanowires upon exposure to ethanol with concentration of 1-200 ppm at 300 °C (reprint permission from ref. [16]); (b) I-V curves of a ZnO nanowire under 0-50 ppm  $O_2$ . Inset: gate potential dependence of sensitivity under 10 ppm  $O_2$ .

#### 7. Optical properties

Intrinsic optical properties of ZnO nanostructures are being intensively studied for implementing photonic devices. Photoluminescence (PL) spectra of ZnO nanostructures have been extensively reported [4, 45-48]. Strong emission peak at 380 nm due to band to band transition and green-yellow emission band related to oxygen vacancy are observed, as shown in Fig. 6a. These results are consistent with those of bulk ZnO. Interestingly, the green emission intensity increases with decreasing nanowires diameter. This observation is attributed to the larger surface-to-volume ratio of thinner nanowires favoring a higher level of surface oxygen vacancy [4]. Recently, Fan *et al.* observed red luminescence attributed to

doubly ionized oxygen vacancies [49]. In addition, as one of the characteristics of nanoscale systems, quantum confinement was observed to cause a blue shift in the near UV emission peak [45] in ZnO nanobelts, as illustrated in Fig. 6b. PL spectra show that ZnO nanowire is a promising material for UV emitting, while its UV lasing property is of more significance and interest. Huang *et al.* [50] and Liu *et al.* [17] reported room temperature UV lasing from ordered ZnO nanowires array (Figs. 6c & 6d). 40 kW/cm<sup>2</sup> and 100 kW/cm<sup>2</sup> lasing power thresholds were reported and the higher threshold was attributed to larger defect concentration present in the wires. As pointed out in ref. 50, the advantages of ZnO nanowire lasers are that the excitonic recombination lowers the threshold of lasing, and in addition quantum confinement yields a substantial density of states at the band edges and enhances radiative recombination.

In addition, well-facetted nanowires form natural resonance cavities, as shown in Fig. 6b. Recently, Law et al. reported using ZnO nanowires as subwavelength optical waveguide [51]. Optically excited light emission was guided by ZnO nanowire into SnO<sub>2</sub> nanoribbon (Fig. 6e). These findings demonstrate that ZnO nanostructures can be the potential building blocks for integrated optoelectronic circuits. Besides UV emitting and lasing, effort on utilizing ZnO nanowires for UV photodetection and optical switching have been reported by Kind et al. [52]. Defect states related visible wavelength detection and polarized photodetection of ZnO nanowires were also observed [49] (Fig. 6f). Photocurrent is maximized when incident light is polarized parallel to nanowire long axis. This behavior is one of the characteristics of Q1D systems and makes them promising application in high contrast polarizer. From the photoconductivity measurements of ZnO nanowires, it is found that the presence of O2 has crucial effect on the photoresponse [16, 49, 53], i.e. O2 surface adsorption on the nanowires could greatly expedite the photocurrent relaxation rate. As shown in Fig. 6g, the photocurrent relaxation time is around 8 s in air but hours in vacuum. It was suggested that photoresponse of ZnO nanowire depends on the desportion-adsorption process of O<sub>2</sub>. Upon illumination, photo-generated holes discharge surface chemisorbed O2 through surface electron-hole recombination, while the photo-generated electrons significantly increase the conductivity. When illumination is switched off, O<sub>2</sub> molecules re-adsorb onto nanowire surface and reduce electron concentration.



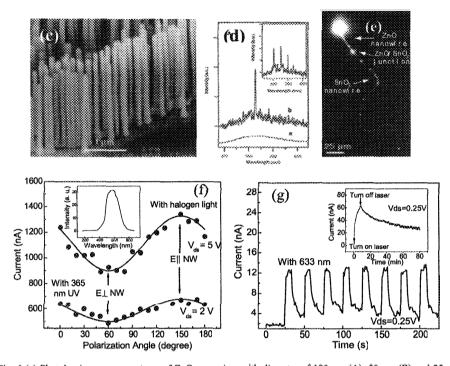


Fig. 6 (a) Photoluminescence spectrum of ZnO nanowires with diameter of 100 nm (A), 50 nm (B) and 25 nm (C) show near UV emission at 380 nm and green-yellow emission band. (reprint permission from ref. [4]) (b) PL spectra of 6 and 200 nm wide ZnO nanobelts show a blue shift of the emission peak. (reprint permission from ref. [45]) (c) Vertical aligned ZnO nanowires array on sapphire substrate used for light emission. (reprint permission from ref. [50]) (d) Emission spectra from nanowire array for optical pumping power below (line a) and above (line b, c) lasing threshold. The pumping power are 20, 100, 150 kW/cm<sup>2</sup>, respectively. (reprint permission from ref. [50]) (e) A PL image of a ZnO nanowire guiding light into a SnO<sub>2</sub> nanoribbon. (reprint permission from ref. [51]) (f) Polarized photodetection of both UV (365 nm) and visible light show that nanowire conductance is maximized when incident light is polarized parallel to the nanowire axis. (g) Nanowire photoresponse to 633 nm laser in air compared to that in vacuum (inset).

#### 8. ZnO nanostructure for spintronics devices

Recently, diluted magnetic semiconductors (DMS) are attracting more and more research effort because spin-polarized DMS can accomplish efficient spin injection. It is found that ZnO is a promising host material for ferromagnetic doping. Room temperature holes mediated ferromagnetic ordering in bulk ZnO by introducing manganese (Mn) as dopant has been predicted theoretically [8] and observed by Sharma *et al.* in ZnO thin film [9]. Ferromagnetism was also observed when Co [54] and Fe [20, 55] were used as dopants. The

effort of growing ferromagnetic  $Zn_{1-x}Mn_xO$  (x=0.13) nanowires with Currie temperature of 37 K was reported by Chang *et al.* [56] and shown in Fig. 7. The nanowires were synthesized via a vapor phase evaporation method. Because of its wide band gap, ferromagnetic ZnO is regarded as an excellent material for short wavelength magneto-optical devices [57]. These studies will pave the way for using magnetic ZnO nanowires as nanoscale spin-based devices, such as spin valves and spin FETs, with the ultimate goal of manipulating a single electron spin rather than the charge as in more conventional devices.

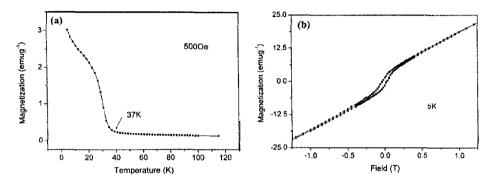


Fig. 7 (a) Temperature dependent magnetization curve of  $Zn_{1-x}Mn_xO$  (x=0.13) nanowire at 500 Oe field shows Currie temperature of 37K. (b) Magnetization-Field hysteresis loop obtained at 5 K demonstrates ferromagnetism by Mn doping. (reprint permission from ref. [56])

#### 9. Summary and future prospects

ZnO offers tremendous potential in providing electronic, photonic, and spin-based functionality. Encouraging progresses on the related research have been achieved as reviewed in this article. There are still important issues waiting to be further investigated, such as growing p-type ZnO nanowires and fabricating nanostructured p-n junction for electrically driven nano LED or laser. Integration of ZnO nanostructures for large scale device applications is another significant issue. Continuous effort will be dedicated to achieving high device density with accessibility to individual nanodevices. Obtaining room temperature ferromagnetism in ZnO nanostructures will greatly advance future research on ZnO based nanoscale spintronics devices.

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#### CARBON NANOTUBE FIELD-EFFECT TRANSISTORS

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This paper discusses the device physics of carbon nanotube field-effect transistors (CNTFETs). After reviewing the status of device technology, we use results of our numerical simulations to discuss the physics of CNTFETs emphasizing the similarities and differences with traditional FETs. The discussion shows that our understanding of CNTFET device physics has matured to the point where experiments can be explained and device designs optimized. The paper concludes with some thoughts on challenges and opportunities for CNTFET electronics.

Keywords: Carbon nanotubes, CNTFET, nanodevice simulation.

#### 1. Introduction

Since the first reports of single-walled carbon nanotubes (CNTs) in 1993,<sup>1,2</sup> they have been the subject of intense interest for basic and applied research. Carbon nanotubes are sheets of graphene (a semi-metal) rolled into a tube.<sup>3</sup> Depending on the way the sheet is rolled up (its chirality) the CNT may be metallic or semiconducting.<sup>3,4</sup> Interest in carbon nanotubes is driven by their exceptional electronic, optical, thermal, and mechanical properties.<sup>3,4</sup> Semiconducting nanotubes are direct bandgap semiconductors with  $E_G \approx 0.8/D$  eV, where D is the nanotube diameter in nanometers. Typical diameters are 1-2nm, and the resulting bandgaps are suitable for room temperature electronics. Low-field transport is near-ballistic with mobilities as high as  $\sim 20,000 \text{ cm}^2/\text{V-s}$  (corresponding mean-free-paths greater than 1 µm).<sup>5,6</sup> The direct bandgap means that they are optically active, so optoelectronic devices are possible.<sup>7,8,9</sup> The conduction and valence bands are mirror images, which is advantageous for complementary circuits. When the first-carbon nanotube field-effect transistors (CNTFETs) were reported in 1998,<sup>10,11</sup> it was not even clear how they functioned, but subsequent progress has been rapid. CNTFET device physics is now rather well understood, and sophisticated transistor structures with high-performance operation are now being reported.<sup>12</sup> Our purpose in this paper is to review the current understanding of CNTFET device physics and to discuss issues and possibilities for future CNTFET technologies.

The paper is organized as follows. In Sec. II, we start with a brief summary of progress in

CNTFET technology since the first reports in 1998. Although it is not a comprehensive review, this discussion is intended to provide background for readers not familiar with CNTFET technology. As our understanding of CNTFET device physics has evolved, an ability to model and simulate them has also been developed. Section III briefly describes the device simulation approach that we use. In Sec. IV, these numerical simulations are used to discuss some key issues in device physics. Unresolved issues and possible applications of CNTFETs are discussed in Sec. V. Finally, we summarize in Sec. VI what we understand, what we still do not completely understand, and what we see as interesting potential applications for CNTFET technology.

#### 2. Background

Manufacturing issues will ultimately play a decisive role in any future CNT electronic technology. Our focus here, however, is on the physics of CNT devices - specifically the CNTFET. It is still too early to tell what role CNTFETs will play in electronic systems of the future, but they provide us with a specific context in which to develop technology and understand transport, contacts, interfaces, etc.; which are likely to be important for CNT electronics in general. It is appropriate, however, to say a few words about where CNTFET technology stands today. Early CNTFETs were fabricated using nanotubes synthesized by a laser ablation process using nickel-cobalt catalysts.<sup>13</sup> The nanotubes were then suspended in a solvent and dispersed on an oxidized silicon wafer with predefined metal contact pads. The result was a random distribution of CNTs with some that bridged the contacts. Subsequently, catalytic chemical vapor deposition (CVD) methods were developed to grow CNTs on predefined catalyst islands.<sup>14</sup> The nanotubes thus fabricated are rooted in the catalyst islands and grow in random directions on the wafer with some terminating on another island creating bridges. CVD techniques provide more control over device fabrication and have led to rapid progress in device performance (e.g. Ref. 12).

CNTFETs are typically p-type devices that operate as so-called Schottky barrier (SB) transistors.<sup>15</sup> The p-type characteristics have been attributed to the alignment of source/drain metal Fermi level near the valance band of the CNTs rather than to background doping or charges.<sup>16</sup> The holes in the channel are electrostatically induced by applying a negative gate voltage. Transistor action occurs because the gate modulates the SB width for hole tunneling near metal-CNT contact.<sup>16,17</sup> While early transistors used gold (Au) as contact metals, significant performance improvements were obtained by using palladium contacts instead, which seem to eliminate the Schottky barrier for holes and produce near-ballistic operation.<sup>18</sup> However, other metals such as cobalt (Co) and titanium (Ti) are still being employed for high performance CNTFETs.<sup>19,20</sup> Metal source/drain FETs, however, still operate differently from the traditional metal-oxide-semiconductor FET (MOSFET).<sup>21</sup> To make a CNTFET operate like a MOSFET, source and drain regions must be created at the two ends of the CNT by heavy doping. MOSFET operation has been reported by using field plates to induce high carrier concentrations in the source/drain extensions.<sup>22,23,24</sup> More recently, CNT MOSFETs with doped source/drain regions have been reported.<sup>25,26,27</sup> It is important to specify the type of CNTFET one is dealing with. We divide them into two broad classes; i) CNT MOSFETs, which are analogous to the traditional silicon MOSFET, and ii) CNT MSDFETs, for metal source/drain FETs. When the Schottky barrier is large, the MSDFET operates as a classic SBFET, and when the SB is small or absent, they operate somewhere between the limits of a MOSFET and SBFET.<sup>21</sup>

Early CNTFETs were fabricated on oxidized silicon substrates with a back-gated geometry and a thick SiO<sub>2</sub> layer that resulted in poor gate control of drain current.<sup>10,11</sup> The use of a top-gated geometry produced immediate performance improvements.<sup>28</sup> Wind et al. deposited a thin dielectric layer (15-20 nm) on top of CNTs, and lithographically defined metal electrodes for gating and contacts. A transconductance  $(g_m = dI_{ds}/dV_{gs}|_{Vds})$  of 3.25 µS and subthreshold swing  $(S = ln(10) [dV_{gs}/d(ln(I_{ds}))])$  of 130 mV/decade were obtained, which was a significant improvement in device performance.<sup>28</sup> Later, the incorporation of high- $\kappa$  dielectrics in a top-gated structure produced even better device characteristics.<sup>29</sup> Javey et al. employed a high- $\kappa$  ZrO<sub>2</sub> ( $\kappa \sim 25$ ) gate dielectric with a thickness of  $\sim 8$  nm and obtained  $g_m \approx 12 \ \mu$ S and S  $\approx$  70 mV/decade.<sup>29</sup> Although not always with top-gated geometry, other groups have also reported the use of high- $\kappa$  dielectrics such as HfO<sub>2</sub> ( $\kappa \sim 11$ ), TiO<sub>2</sub> ( $\kappa \sim 40-90$ ), SrTiO<sub>3</sub> ( $\kappa \sim$ 175), and even-electrolyte gating mechanisms for attaining improved performances.<sup>17,20,30,31,32</sup> In the case of electrolyte gating, Siddon et al. have reported  $S \approx 62$  mV/decade which is very close to the theoretical limit of 60 mV/decade.<sup>32</sup> All of these devices appear to operate as CNT MSDFETs, some with essentially no barrier and others with rather large (half bandgap) barriers.

The possibility of ballistic operation of CNTFETs has been a topic of great interest. Since there are no dangling bonds in CNTs, surface scattering can be expected to be negligible. Back-scattering by acoustic phonons is suppressed by symmetry arguments related to the CNT bandstructure<sup>33,34</sup> and by the reduction in phase space for one-dimensional conductors. The result is that mean-free-paths of several hundred nanometers are commonly observed.<sup>33,35</sup> Under high bias, however, optical or zone boundary phonons may be emitted, and the mfps decrease substantially. Yao et al. showed that for long metallic CNTs, the current saturates at about 25  $\mu$ A per nanotube.<sup>33</sup> They showed that the high-field current is limited by the emission of optical or zone boundary phonons with  $\hbar\omega_0 \approx 200$  meV and that the high-field mfp is ~ 10nm. Yao's results suggest that for short nanotubes, comparable in length to the mfp, the current should exceed 25  $\mu$ A per nanotube. This expectation was confirmed by Park et al<sup>36</sup> and Javey et al.<sup>35</sup> who both showed that the current increases above 25  $\mu$ A when the length of the nanotube is less than several mfps long. By analyzing their data, both Park and Javey extracted an mfp of  $\sim 10 - 15$  nm, which was consistent with the value extracted by Yao for long nanotubes. The mfps deduced from these experiments are considerably shorter than the values of 50nm or so, which are estimated from the expected electron-phonon coupling strength.<sup>33,36</sup> Although these results are for metallic nanotubes, similar effects are expected for semiconducting nanotubes and CNTFETs. For a tube much shorter than the mfp, carrier transport in the tube is quasi-ballistic, and the tube resistance is nearly length-independent. In contrast, a tube much longer than the mfp behaves like a classical resistor, in the sense that the resistance is proportional to the tube length.

Several recent improvements to CNTFET design collectively incorporate various techniques that have been developed during the past few years. For instance, Javey et al. reported a self-aligned top gate structure that uses the catalytic CVD method for CNT growth, a thin  $HfO_2$  top gate dielectric ~ 50 nm in length and self-aligned palladium source/drain contacts.<sup>12</sup> A transconductance of 30  $\mu$ S, subthreshold swing of 110 mV/decade, and a saturation current of ~25  $\mu$ A at a power supply of V<sub>DD</sub>~1V were obtained.<sup>12</sup> Novel CNTFET device structures that enable high current operation <sup>37</sup> and high integration densities <sup>38</sup> have also been reported. These devices are all of the metal source/drain (MSDFET) variety, but it is recognized that the use of a metal source will limit the drain current (unless the SB is sufficiently negative).<sup>21</sup> Very recently, CNT MOSFETs with doped source/drain regions have been reported.<sup>24-27</sup> Substitutional doping is not practical because of the strong carbon-carbon bond, so charge transfer approaches analogous to modulation doping in III-V heterostructures <sup>26,27,39</sup> are used. Although progress in CNTFETs has been rapid, there are still many issues to address. The potential for digital logic 40,41 was demonstrated early on. Techniques that modify the behavior of the nanotube from p-type to n-type have been implemented, which allowed their use in complementary CMOS logic. Following this, Derycke et al. demonstrated an inverter structure based on nanotubes.<sup>40</sup> Other nanotube based elementary digital logic gates with high gain and high I<sub>or</sub>/I<sub>off</sub> ratios, such as a NOR gate, a ring oscillator and an SRAM cell, have also been implemented.41

With respect to RF performance, measurements <sup>42-44</sup> and modeling <sup>45-47</sup> have both been initiated to assess performance potential. Experimental work includes that of Frank and Appenzeller,<sup>42,43</sup> who developed a technique to circumvent the low-current-drive problem of CNTFETs to place a lower bound on the frequency response. Li et al.<sup>44</sup> measured the microwave reflection coefficient from a load comprised of a nanotube and a matching circuit and demonstrated transistor operation at 2.6 GHz. In terms of modeling, Burke <sup>45,46</sup> has suggested an RF circuit model for a metallic nanotube, and emphasized the importance of both quantum capacitance and kinetic inductance. More recently,<sup>47</sup> Burke used a standard formula, along with estimated and measured values for the parameters, to predict the unity-current-gain frequency ( $f_T$ ) of CNTFETs, and suggested the  $f_T$  would be given by 80 GHz divided by the tube length in microns [ $f_T = 80 GHz / L(in \mu m)$ ]. However, as we discuss near the end of this paper, much more needs to be done to definitively characterize the RF behavior of CNTFETs.

A pressing issue that limits logic and RF device performance has to do with contacts. Good contacts to the valence band are achieved by using palladium. The barrier height is approximately zero for relatively large diameter nanotubes  $(D \sim 1.7 \text{ nm})$ . Achieving small barrier contacts to the small diameter nanotubes that will be necessary for room temperature operation  $(D \sim 1\text{nm})$  is a key challenge, as is also achieving good, low barrier, contacts to the conduction band. CNT MOSFETs, however, are expected to deliver significantly better performance than MSDFETs, and recent progress on stable, heavy doping of CNTs is encouraging.<sup>25,26,27</sup> For many (perhaps most) applications, high currents are needed, so innovative structures that place several CNTs in parallel will be required. If these problems can be addressed, manufacturing challenges will move to the forefront. The key challenges are control of chirality and development of low temperature growth processes to allow CNTFETs to be placed at low cost on CMOS substrates. For the remainder of this paper, our focus will be on the physics of CNTFETs. Before we examine device physics, we first describe the simulation techniques that we use to explore and understand device physics.

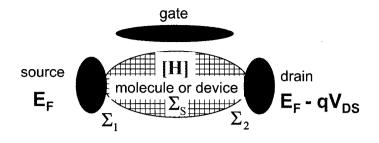


Fig. 1. A generic transistor comprised of a device channel connected to source and drain contacts. The source-drain current is modulated by a third electrode, the gate. The quantities involved in the NEGF formalism are also shown.

#### 3. CNTFET Device Simulation by the NEGF Approach

A number of groups have reported modeling and simulation studies of CNTFETs (some examples are Refs. [17], and [47-53]). Our intent in this section is not to review that work. Instead, we briefly describe the techniques we currently use to simulate CNTFETs, because the results of our simulations will be used in Sec. 4 to illustrate key features of CNTFET device physics.

Detailed treatment of carbon nanotube electronics requires an atomistic description of the nanotube along with a quantum-mechanical treatment of electron transport. For ballistic transport, we self-consistently solve the Poisson and Schrödinger equations using the non-equilibrium Green's function (NEGF) formalism.<sup>54</sup> To test the validity of the simulation, we compare simulated results to a recently-reported CNTFET.<sup>12</sup> The comparison shows that the self-consistent quantum simulation captures the essential physics of the CNTFET. Electron-phonon scattering does occur under modest bias <sup>35</sup> and can be simulated by semiclassical, so-called Monte Carlo techniques,<sup>55</sup> but scattering has a rather small role on the dc performance of CNTFETs with a channel length less than 100nm.<sup>56</sup>

To correctly treat transport in carbon nanotube transistors, we need to include quantum mechanical tunneling through the Schottky barriers at the metal-nanotube contacts, and quantum tunneling and reflection at the barriers within the nanotube channel. The non-equilibrium Green's function (NEGF) formalism provides a sound approach to describe ballistic and dissipative quantum transport.<sup>54,57</sup> Figure 1 describes the essence of the technique and the key parameters of the formalism. The approach begins by identifying a suitable basis set and Hamiltonian matrix for the isolated channel. The self-consistent potential, which is a part of the Hamiltonian matrix, is included in the diagonal components of **H**, which is an  $N \times N$  matrix where N is the total number of orbitals in the simulation domain (i.e. the number per carbon atom times the number of carbon atoms in the channel). The second step is to compute the so-called self-energy matrices,  $\Sigma_1$ ,  $\Sigma_2$ , and  $\Sigma_S$ , which describe how the channel couples to the source and drain contacts, and to the scattering process. For simplicity, only ballistic transport is treated in this paper, so  $\Sigma_S \equiv 0$ . The third step is to compute the retarded Green's function,

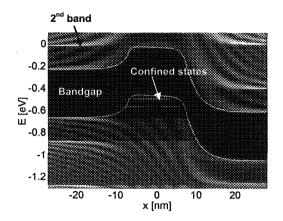


Fig. 2. The computed local density of states for a CNTFET under high gate and drain bias. Light areas indicate a high density of states.

$$\mathbf{G}(E) = [(E+i0^{+})\mathbf{I} - \mathbf{H} - \boldsymbol{\Sigma}_{1} - \boldsymbol{\Sigma}_{2}]^{-1}.$$
 (1)

The fourth step is to determine the physical quantities of interest from the  $N \ge N$  Green's function matrix. For example, the position-resolved electron density in the device is

$$n(z) = \int dE \left\{ LDOS_1(x, E) f_1(E) + LDOS_2(x, E) f_2(E) \right\},$$
(2)

where  $f_{1,2}$  the equilibrium Fermi functions of the two contacts, and  $LDOS_{1,2}$  is the local density of states fillable by contact 1 or contact 2, which are obtained from the retarded Green's function [eqn. (1)]. For a self-consistent solution, the NEGF transport equation is solved iteratively with the Poisson equation until self-consistency is achieved. After that the source-drain current is computed from

$$I = \left(\frac{4e}{h}\right) \int T(E) [f_1(E) - f_2(E)] dE , \qquad (3)$$

where  $T(E) = \text{Trace}(\Gamma_1 G \Gamma_2 G^+)$  is the transmission between the source and the drain,

 $\Gamma_{1,2} = i \left( \Sigma_{1,2} - \Sigma_{1,2}^{+} \right)$ , and the extra factor of two in (3) comes from the valley degeneracy in

the carbon nanotube energy band structure.

The NEGF approach as described above can be implemented by using an atomistic basis set that consists of the  $p_Z$  orbitals of all the carbon atoms in the channel. This approach produces a matrix whose size is the total number of carbon atoms in the nanotube, which makes it computationally intensive. Figure 2, which plots the computed local-density-of-states (*LDOS*) at on-state, shows that the simulation captures all important quantum effects. A mode-space

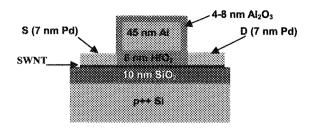


Fig. 3. A recently reported CNTFET with Pd source and drain contacts and a 50nm-long channel.<sup>23</sup> The HfO<sub>2</sub> top-gate insulator is 8nm thick with a dielectric constant  $\kappa \approx 16$ . The diameter of the intrinsic carbon nanotube channel is  $d_{CNT} \approx 1.7$  nm. The Pd source and drain contact thickness is 7nm.

approach that significantly reduces the size of the Hamiltonian matrix when the potential around the tube is nearly invariant has also been developed.<sup>56</sup> It is similar to an approach that has been used for nanoscale MOSFETs.<sup>58</sup> It is exact for coaxially gated CNTFETs, and it also applies to CNTFETs with planar gates when the potential variation around the tube is small compared to the subband energy spacing. In brief, the idea is to exploit the fact that in a carbon nanotube, periodic boundary conditions must be applied around the circumference of the nanotube, so transport can be described in terms of these circumferential modes. Mathematically, we perform a basis transformation on the (n, 0) zigzag nanotube to decouple the problem into n one-dimensional mode-space lattices. Since only a few modes are typically involved in transport, the size of the problem is dramatically reduced, and routine device simulation and optimization becomes possible. See Refs. 56 and 59 for a detailed discussion of this approach.

In addition to the NEGF treatment of carrier transport, the device simulation requires that it be coupled to a solution of Poisson's equation for self-consistent electrostatics. Details of the electrostatic solution and coupling to the transport equation are discussed in Ref. 59. Most

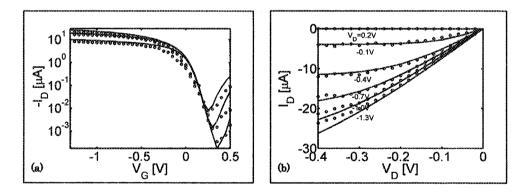


Fig. 4. Experimental (circles) and simulated (solid lines) (a)  $I_D$  vs.  $V_G$  at  $V_D$ =-0.1, -0.2, and -0.3V and (b)  $I_D$  vs.  $V_D$  characteristics. The CNT work function  $\Phi_{CNT}$  = 4.7 eV, the Al top-gate work function  $\Phi_{AI}$  = 4.1 eV, and the p<sup>+</sup> doped bottom-gate work function  $\Phi_{pSi}$  = 5.1 eV. No interface and oxide charges are included. The simulated  $I_D$ -V<sub>G</sub> curves are translated by +0.75V along the x-axis to match the experimental curves.

CNTFETs contain a Schottky barrier at the source and drain. An atomistic treatment of the contact is not practical for device simulation, so a phenomenological treatment has been developed.<sup>56,59</sup> The overall technique has been used to simulate a recently-reported CNTFET as shown in Fig. 3.<sup>12</sup> A self-aligned gate process was used to achieve a channel length of 50nm with a D = 1.7nm CNT. A high- $\kappa$  top gate insulator was used to maximize the gate modulation, and low-barrier contacts ( $\Phi_{bp} \approx 0$ ) to the valence band were used at the source and drain to optimize the metal-nanotube contacts. This transistor demonstrates excellent on-state performance with  $I_D \sim 20 \ \mu$ A and a near-ideal channel conductance of  $0.5 \times 4e^2 / h$  achieved at a gate overdrive  $|V_{G} - V_T| \sim 1V$ . Figure 4 plots the experimental (circles) and theoretical (lines) current-voltage characteristics. The parameters used in the quantum simulation were obtained from separate electrical measurement and characterization. The results show that the simulation is adequate to model the experimentally measured current-voltage characteristics. In the next section, we will use numerical simulations to discuss the physics of CNTFETs.

#### 4. Device Physics of CNTFETs

Much has been learned about the device physics of CNTFETs since their first demonstration only a few years ago; our objective in this section is to summarize our current understanding of CNTFET device physics. Figure 5 illustrates two different ways to make a transistor. In the traditional MOSFET (Fig. 5a), the source and drain regions are heavily doped and an electrostatic potential barrier that prevents current flow occurs in the channel. A positive gate voltage pushes the barrier down and allows current to flow. In the so-called Schottky barrier FET (Fig. 5b), the source and drain contacts are metallic. Below threshold, the potential barrier in the channel looks much like that in a MOSFET, but above threshold, a Schottky barrier exists between the source and the channel. Transistor action occurs because the gate voltage modulates the tunneling current by modulating the width of the barrier. Because there is a tunneling barrier at the source, one should expect the on-current of a Schottky barrier FET

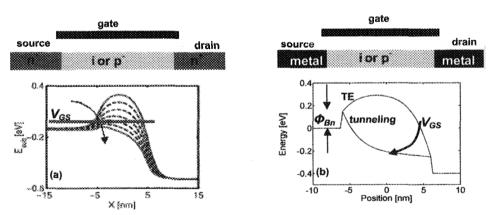


Fig. 5. Illustration of two kinds of transistors. (a) the traditional MOSFET, and (b) a metal source/drain (or Schottky barrier) FET.

to be lower than that of a traditional MOSFET. Metal contacts with essentially no barrier to the valence band can be produced (the Pd-CNT contacts of Javey et al.<sup>18</sup>), but it is not enough to reduce the barrier height to zero, because even then a significant fraction of the current is carried by electrons below the Fermi level which must tunnel into the semiconductor.<sup>21</sup> In fact, for a typical MOSFET, the Fermi level in the  $n^+$  source and at the beginning of the channel is well above the conduction band, which is effectively a negative Schottky barrier.<sup>21</sup> Because metal source/drain FETs may operate with or without an actual Schottky barrier, we prefer the more general term, metal source-drain FET (MSDFET) for such devices.

Figure 6a shows the (simulated) I-V characteristics of the type that are typically observed for MSDFETs with mid-gap Schottky barriers. For  $V_{GS} > V_{DS}/2$ , the device is a Schottky barrier FET that operates by electron tunneling, but for  $V_{GS} < V_{DS}/2$ , it is a Schottky barrier FET that operates by hole tunneling. The energy band diagram at  $V_{GS} = V_{DS}/2$  (Fig. 6b) shows that the device is symmetrical at this bias: electron tunneling with the left contact as the electron source, (with  $V_{GS} = +V_{DS}/2$ ) and hole tunneling with the right contact as the hole source (with  $V_{GS} = -V_{DS}/2$ .). Strong tunneling occurs in these devices because of the small effective mass and the thin barriers.

The minimum current of a SB CNTFET can be shown to be 60

$$I_D = \frac{8ek_BT}{h} \langle T \rangle e^{-(E_G - qV_{DS})/2k_BT}, \qquad (4)$$

where  $\langle T \rangle$  is the average current transmission coefficient. Ambipolar FETs can be used for digital logic, but the leakage current increases the standby power.<sup>61</sup> Acceptable leakage currents require a bandgap of at least ~0.8eV (a nanotube diameter of less than 1 nm). Another possibility for suppressing ambipolar conduction is to use a metal with a small barrier to the conduction band for the n-FET and another metal with a small barrier to the valence band for the p-FET. This approach is not very successful because the small effective masses and thin barriers produce strong tunneling.<sup>62</sup> Thick gate insulators lead to thick barriers that do suppress ambipolar conduction when the Schottky barrier is off mid-gap, but thick gate insulators lead to poor FET performance.<sup>62</sup> Clever ideas that produce a thick oxide at the drain end and a thin one at the source have been explored,<sup>63</sup> but it is not clear how manufacturable

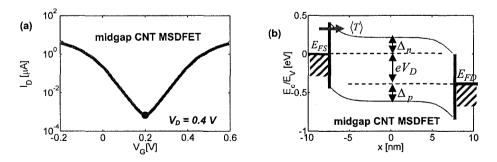


Fig. 6. Operation of a mid-gap Schottky barrier transistor. (a) the log  $(I_D)$  vs.  $V_{GS}$  characteristic, and (b) the energy band diagram at  $V_{GS} = V_{DS}/2$ .

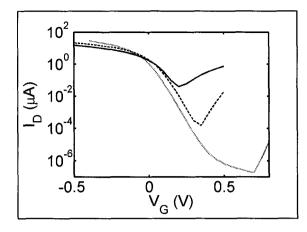


Fig. 7. The log( $I_D$ ) vs.  $V_{GS}$  plots comparing of three type of CNTFETs sat  $V_{DS} = 0.4$ V. Solid line: the CNT MSDFET device of Javey et al.<sup>12</sup> Dashed line: simulation of a similar CNT MSDFET but with a small diameter nanotube (1.0 nm instead of 1.7 nm) and a thinner HfO<sub>2</sub> gate insulator (4nm instead of 8 nm). Dotted line: Simulation of a CNT MOSFET with the same nanotube diameter and gate insulator as in the dashed line.

such approaches would be.

The achievement of carbon nanotube MOSFETs would provide improved on-current and suppress ambipolar conduction. Figure 7 illustrates what may be possible; it compares a recently reported p-type MSDFET in which the barrier to the valence band is approximately zero <sup>12</sup> to two simulations. The first simulation is for a MSDFET similar to <sup>12</sup> but with a smaller nanotube (D = 1.0nm) and thinner gate insulator (4 nm of HfO<sub>2</sub>). (For this simulation, we assume that a barrier height of zero to the valence band can still be achieved in the smaller diameter nanotube.) The second simulation is for a CNT MOSFET with the same diameter nanotube and the same gate insulator. The CNT MOSFET is seen to offer higher on-current and lower off-current. Ambipolar conduction is also observed in the CNT MOSFET, but it occurs by band to band tunneling and is orders of magnitude lower. To achieve such devices, we must learn how to efficiently dope CNTs. Substitutional doping is difficult to envision because of the strong carbon-carbon bonds, so charge transfer schemes analogous to modulation doping in III-V semiconductors is being explored. Promising results have recently been reported<sup>25-27</sup> and more work is underway.

The interest in CNTFETs was spurred by the demonstration of exceptionally high mobilities in CNTs.<sup>5,6</sup> Under low bias, mean-free-paths of several hundred nanometers are observed. As discussed earlier, however, under high bias optical and zone boundary phonons can be emitted, and the mean-free-path decreases to about 10 nm. One might expect that these short of mfps would degrade the on-current of a CNTFET, but recent simulations show that this is not the case.<sup>56</sup> Because the optical phonon energy is so high (~200 meV), a carrier that backscatters by emitting an optical phonon does not have sufficient energy to surmount the barrier and return to the source.<sup>56</sup> Such carriers rattle around in the channel and diffuse out to the drain. The result is that the steady-state drain current is not affected by such scattering and the dc current is essentially at its ballistic value.

#### 5. Discussion

During the past few years, much has been learned about the physics of CNTFETs. Sophisticated device structures with high- $\kappa$  gate dielectrics and self-aligned gate electrodes are now being reported.<sup>12</sup> Contacts are still a challenge, especially low barrier contact to the conduction band. Techniques to achieve stable, high levels of doping will need to be developed so that high performance CNT MOSFETs can be produced. Our understanding of scattering is still incomplete; for example, the mean-free-paths computed from the expected electron-phonon coupling parameters <sup>36,64</sup> are longer that the value deduced from experiments.<sup>33,35,36</sup> Hot phonon effects, which are a possible explanation for this discrepancy, need to be explored. Scattering in doped CNTs is also not understood. Javey et al.<sup>29</sup> observed good transport properties after the tube is very heavily doped, but Appenzeller et al.<sup>65</sup> observed a significant degradation of current due to doping. The future of CNTFETs will depend on two things, finding appropriate applications and developing high volume manufacturing technologies.

Because of their excellent transport properties, RF applications of CNTFETs have been the subject of considerable recent interest.<sup>43,44</sup> While the dc performance of CNTFETs is now understood rather well, little is known about their RF performance. The band-structure limited velocity of  $\sim 8x \ 10^7$  cm/s is high and leads to expectations of THz performance. We have argued that phonon scattering has a small effect on the dc current of a CNTFET, but it does lead to dispersion in the transit time and should affect the ac performance. For RF applications, the MSDFET may be suitable, because leakage currents are not as important as in high density digital circuits. We still do not understand, however, how CNT MSDFETS and CNT MOSFETs compare for high-frequency applications. Other issues, such as the role that the so-called kinetic inductance <sup>45,46</sup> might play in such devices, also need to be explored.

#### 6. Summary

Carbon nanotube field-effect transistors are interesting devices with potentially important applications in electronics. In this paper, we have summarized the current status of the field in terms of fabrication technology and device physics. The rate of progress in CNTFET technology and in the understanding of their device physics has been very rapid. Although uncertainties remain, the dc performance of field-effect transistors can now be explained. During the next few years, we expect to see increased work on other devices, for example, high-speed transistors, optoelectronics devices, and bio-sensors. We are sure to learn a good deal of interesting new device physics in the process and may even discover important technological applications.

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## **Carbon Nanotube Based Microwave Resonator Gas Sensors**

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This paper reviews our work on the development of microwave carbon nanotube resonator sensors for gas detection. The sensor consists of a radio frequency resonator coated with a layer of carbon nanotubes. Upon exposure to gasses, the resonant frequency of the sensor shifts to indicate the presence of gasses. Our experimental results demonstrate that the microwave carbon nanotube resonator sensor achieves a sensitivity of 4000 Hz/ppm upon exposure to ammonia and the resonant frequency is recovered when ammonia is evacuated. The sensing mechanism is dependent on electron transfer from the ammonia to the nanotubes. This sensor platform has great potential for wireless sensing network applications.

Keywords: carbon nanotubes, wireless, sensor, and remote.

## I. Introduction to Carbon Nanotube Gas Sensors

Chemical sensors are currently one of the most important research areas. The ability to monitor our environment is becoming increasingly important. With the world market for sensor microsystems estimated to be greater than \$38 billion<sup>1</sup>, the current demand is already extraordinary with many applications yet to be realized. From improving the efficiencies of industrial processes, to monitoring changes in our planet's ecosystem, and to ensure national security the possibilities for reliable, sensitive, compact, and cost efficient sensors are overwhelming. Despite many difficulties, the recent successes in the field carbon nanotube chemical and biological sensors offer excellent promise in the near future.

Gas sensors have various implementations. The most common implementation to date is the semiconductor sensor. Semiconductor sensors use the charge transfer from/to an impurity to/from the transducing material (the semiconductor). This causes a change in the carrier concentration which manifests itself as a resistance change in the material. Metal oxides are the most commonly used material with the main disadvantage being that they require relatively high temperatures (~200  $C^{0}$ )<sup>2-10</sup>. Another technique receiving a fair amount of attention in recent years is the surface acoustic wave (SAW) sensors. Although implemented on a platform suited for wireless applications, demonstrations of its utility as a gas sensor have not been compelling due to low sensitivity<sup>11-23</sup>. Other techniques used for gas sensing include optical fibers terminated or coated with a sensing material, infra-red spectroscopy, and various mass spectroscopy techniques currently used in laboratories. Although these methods are very precise, their size and cost prohibit them from wide acceptance<sup>24-28</sup>. Another technique similar to semiconductor sensors is the use of nano-structured sensors. Most of the nano-structured materials used are also semiconductors. Currently, three of the most popular materials are nanobelts<sup>10</sup> (suffering from the same temperature restrictions as metal oxides), nanowires, and carbon nanotubes, the subject of this paper.

Nanotechnology can offer solutions to scalability, integration, and sensitivity issues that have plagued traditional technologies- a fact that was already recognized by Gopel in 1991<sup>29</sup>. In nanomaterial based sensors, sensitivity increases of six to eighteen orders of magnitudes are theoretically and practically possible. The detection of single molecules by Cu nanowire based sensors has already been reported<sup>30</sup>. Sensing will also become much faster. By introducing transducers with nanoscale dimensions, the lengths of electrical connections are decreased, and sensing speeds can be increased substantially. Nanoscale phenomena such as conductance quantization<sup>31</sup> and single electron charging<sup>32</sup> will be utilized for sensing purposes. The required techniques (scanning tunneling microscopy (STM), atomic force microscopy (AFM), near-field scanning optical microscopy and laser spectroscopy) for the detection of these novel phenomena are already available.

Particular interest exists in using nanowires of semiconducting and metallic<sup>33, 34</sup> materials as sensor elements. The advantage of these one-dimensional electrical conductors is that they can be employed for both detection and signal transduction. Chemically modified and non-modified nanowires for biochemical and gas sensor applications were fabricated by Yang<sup>35</sup> and Lieber<sup>36</sup>.

Similar applications have been realized with carbon nanotubes. As shown by Dai and coworkers, <sup>37</sup> gases such as NO<sub>2</sub> can change the electrical conductivity of carbon nanotubes by three orders of magnitude even at a concentration of only 20 ppm. Collins<sup>38</sup> obtained similar results when exposing carbon nanotubes to oxygen. These reported sensitivities, as well as very short response times, exceeded the performance of comparable solid-state sensors.

Nano-structured materials have been used as the sensing material in three main categories of sensors: the SAW sensor<sup>11, 15-22</sup>, conductivity sensors, and spectral domain sensors. SAW sensors, as mentioned above, suffer from the drawback of low sensitivity. Conductivity sensors, on the other hand, have relatively high sensitivity and have been used with a wide range of materials<sup>2-10, 36-52</sup>. Conductivity sensors operate at DC and have two common implementations. The first is simply using the sensing material as a resistor, and the second involves using the material as the channel of a FET. Upon exposure to impurities, the material will change its conductivity, which will be sensed as either a current or voltage change. Conductivity sensors have been used with a wide range of materials. Metal oxides have had much success in gas sensing<sup>2-10</sup>, but due to the temperature requirement, they are not suited for wireless applications. Conductive polymers<sup>43, 52-53</sup> and carbon nanotubes<sup>37-41, 44-51</sup> have been demonstrated to operate at room temperature, and the use of mass selective polymer coatings<sup>53</sup> offers potential of improving the sensitivity of nanotube based sensors. The essential drawback with these sensors is their response time, which improves with temperature<sup>54</sup>.

Spectral domain sensors<sup>55-66</sup> are very similar to conductivity sensors, except that changes in conductivity at a frequency or over a range of frequencies are used to determine the concentration of impurities. These structures can simply be conductivity devices operated at higher frequencies, where the concentration of the impurities would be deduced from the changes in the ac transfer characteristics of the material<sup>63</sup>. They can also be capacitors, planar inductors<sup>56</sup>, microwave resonators<sup>39-40, 58-63</sup>, or simply a terminated transmission line<sup>55</sup>. The choice of where to put the sensing material on these structures depends on where it will have the greatest effect on performance when its properties change as well as where it will be the most exposed to the environment. Spectral domain sensors offer one significant advantage over conductivity sensors in that they can operate at a frequency suited for wireless transmission. Thus, impedance sensors are capable of creating wireless sensor nodes with minimal complexity, as shown by Yoon<sup>55</sup> and Kong<sup>56</sup>.

The remainder of this paper of consists of six sections. First we will present a brief review of sensor terminology. Second, we will discuss the electrical properties of carbon nanotubes, as well as a brief explanation of the sensing mechanism. Third, we will describe the work we have done at U.C. Davis, providing a summary of our design process, experimental setup, experimental results, and further discussion regarding the sensing mechanism. The remaining sections will review recent developments in wireless gas sensing nodes, functionalizing carbon nanotubes for specific applications, and, finally, describe our future research in the development of the microwave carbon nanotube resonator sensors.

## II. Review of Gas Sensor Terminology

Gas sensors must meet a variety of criteria in order to be practical. The sensor must respond within a relatively short time period to give an accurate assessment of the current impurity concentration. Response time is usually used to specify the time interval required for the sensor to stabilize at its final value. Other terms are sometimes used to characterize the response time such as rise time. This term is used to characterize the time required for the sensor response to reach a certain percentage of its final value.

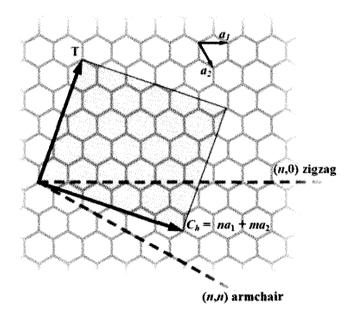
Sensors should also be reusable for wide acceptance. The characterization of how long the sensor takes to return to its initial state is its recovery time. Recovery time generally refers to the amount of time required for the sensor to stabilize at its initial state. Fall time (or rise time depending of the sensors response) may also be used and refers to the time interval required for the sensor to return to some percentage, usually ninety, of its initial state. Recovery is one of the main obstacles of carbon nanotube based sensors, which can take several hours.

Sensitivity is used to characterize the change in the sensor's response for a given concentration of gas. Obviously, the amount of changes for a given concentration of gas is of primary importance. In this paper sensitivity will refer to the sensor response, characterized by frequency shift, divided by the concentration in ppm. The linear range of the sensor response corresponds to a range of concentrations for which the sensitivity is constant. Linearity in the response is desirable. However, as long as the response is monotonic, and repeatable, this is not a major concern. Another parameter related to sensitivity is selectivity. Not only must the sensor be highly sensitive, but it must be sensitive only to the impurities of interest to avoid false alarms.

# III. Properties of Carbon Nanotubes and Mechanisms for Gas Sensing

Carbon nanotubes have very high aspect ratios and are essentially all surface area. The two main aspects of nanotubes that determine their electrical properties are diameter and chirality. If the nanotube is envisioned as rolled graphite sheet, the tube's chirality is determined by how the sheet attaches to itself. The chiral vector is defined as  $C_k=n\times a_1+m\times a_2$  (see Figure 1.) and is between two equivalent sites representing where the graphite sheet attaches to itself to form the nanotube. The vector is directed along the circumference of the

tube and normal to its axis. The magnitude of the vector is equal to the diameter of the tube, while its direction indicates its chirality. Carbon nanotubes have three distinct categories classifying their chirality: armchair, zig-zag, and chiral tubes. Zig-zag and armchair tubes are referred to as achiral tubes, while all other tubes are chiral tubes. Tubes are also classified as being either metallic or semi conducting. All armchair tubes, described by n=m, are metallic. Zig-zag tubes, described by m=0, are metallic if n is a multiple of three. The condition for a nanotube to be conducting can be stated as the difference between n and m must be a multiple of three or zero. The conditions for the nanotubes to be metallic are equivalent to the chiral vector intersecting the points were valence and conduction bands in the first brillouin zone of the equivalent graphite sheet are degenerate, and, therefore, no band gap occurs. For the tubes having a band gap, the band gap is inversely proportional to the diameter of the tube<sup>70</sup>.



# Figure 1. Illustration of the chiral vector( $C_h$ ) in terms of vectors $a_1$ and $a_2^{68}$

Nanotube sensors rely on the transfer of charges from the species to be detected to the nanotubes. Conductivity sensors measure this directly. The charge transfer either increases or decreases the number of free carriers<sup>38, 41, 44-51</sup> and the number of free charge carriers is linearly proportional to the conductivity. The change depends on the state of the tubes and the direction of charge transfer. Most nanotubes are p-type due defect sites, where the defect sites have been proposed to dope the nanotubes p-type through oxygenation<sup>38, 41</sup>. Oxidizing species accept electrons, increase the number of holes, and thus increase the

conductivity. Reducing species donate electrons to the tubes, tend to fill the holes, and reduce the conductivity<sup>72</sup>. Spectral domain sensors, the subject of this paper, involve monitoring the impedance of the sensing structure. In the sensor presented here, impedance is monitored by observing the magnitude of the insertion  $loss(S_{11})$  of a microstrip resonator, coated with carbon nanotubes. The frequency of resonance, determined by the electrical permittivity of the nanotube coating, indicates a relative concentration of impurities. The frequency of resonance can be determined by the sharp dip in the S<sub>11</sub>, indicating that energy is transmitted to the resonator with little or no reflection. In the work of Yoon et al<sup>55</sup>, the phase of S<sub>11</sub> of a carbon nanotube terminated coplanar waveguide is used for detection. In Kong et al<sup>56</sup>, the impedance of a planar tank circuit, coated with carbon nanotubes, is monitored around 10MHz.

### IV. Wireless Carbon Nanotube Gas Sensor

### 4.1 Sensor Design

The microwave circular disk resonator was designed on a Duroid board (RO4350B) that has a dielectric constant of 3.48 and a thickness of  $\sim 1.5$  mm. The resonant frequency was first determined by an approximate formula for the resonant frequency at the dominant mode:

$$f_0 = \frac{1.841c}{2\pi a \sqrt{\varepsilon_r}}$$

where  $f_0$  is the resonant frequency of the resonator, c is the speed of light in vacuum, a is the radius of the disk,  $\varepsilon_r$  is the relative dielectric constant of the substrate (Duroid board). The resonator can be scaled to higher frequency to achieve greater sensitivity and reduce device size. Capacitive gap was designed to couple RF electromagnetic energy in and out of the circular disk resonator. A 50- $\Omega$  transmission line was used to feed RF signals into the resonator with a gap of ~200 $\mu$ m. The resonator has a radius of 7.5mm and the resonant frequency of sensor is ~5.5GHz. The dimensions of the gap were designed so that the return loss at resonant frequency is beyond 20 dB. The Sonnet<sup>®</sup> electromagnetic tool was used to optimize the capacitive gap for optimum impedance at the resonant frequency. A 3.5 mm connector was soldered to the other end of the microstrip line to provide connection to a microwave vector network analyzer.

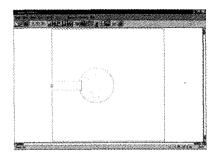


Figure 2. Model used in Sonnet<sup>®</sup>simulation

Single wall carbon nanotubes (SWNTs) and multi-wall carbon nanotubes (MWNTs) can be assembled on top of the resonator disk to form a transducer for gas sensing. The microwave carbon nanotube resonator sensor is configured in a 1-port device of which the frequency response return loss or reflection coefficient will be used to determine the resonant frequency. Figure 3 shows a diagram of the microwave carbon nanotube resonator sensor and its cross section. In our current design, we employ single wall carbon nanotube powder purchased from Carbon Nanotechnologies Incorporated<sup>71</sup>. The single wall carbon nanotubes have diameters ranging from .8 to 1.2 nm with the average being 1nm. The lengths of the nanotubes range from .8nm to 10000 nm. The single wall carbon nanotube power is purified to 14% Fe by weight. The carbon itself is 95% nanotubes and the rest consist of amorphous carbon and partial fullerene structures. The nanotubes are roughly a third conducting, a third semi conducting, and a third insulating. The carbon nanotubes were applied to the copper disk by applying a thin layer of conductive epoxy and pressing the nanotube powder on top of The result is a dense, thin layer of randomly orientated tubes with a high number the epoxy. of defect sites due to pressing the nanotubes. The thickness of the carbon nanotube is -5 - 10The application of carbon nanotubes and conductive epoxy to the surface of the um. resonator causes degradation in the performance of the resonator which necessitates manual Figure 4 shows a picture of an actual prototype. tuning of the structure afterwards.

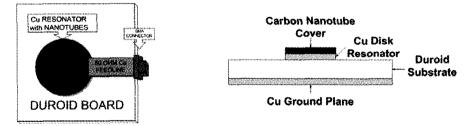


Figure 3. Diagram of Microwave Carbon Nanotube Resonator Sensor and its cross section.

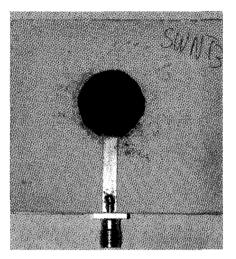


Figure 4. Picture of a prototype

## 4.2 Experimental Set-Up

Figure 5 shows the testing set-up for measuring the microwave carbon nanotube resonator sensor. The testing chamber has an RF feed-through coax cable to provide high frequency testing signals to the sensor. The sensor prototype is placed inside the testing chamber and is monitored using an 8364B Agilent Performance Network Analyzer (PNA). Due to the degradation in the performance of the resonator from the application of the carbon nanotubes, an impedance tuner was used to match the resonator and coax feed line to 50 Ohms at the resonant frequency. The PNA has a measurement resolution of 312 KHz. The network analyzer is used to measure the transfer function of the one-port resonator device to determine the resonant frequency. The transfer function, in this case, the ratio of the input RF power and the return power. Before the measurements, the PNA was calibrated using short-open-load-thru calibration (SOLT). The Agilent 8505C APC7 calibration standards were used. The ammonia gas was supplied to the testing chamber using a Unit UFC 1100A mass flow controller (MFC), which was calibrated by Coastal Instruments for 0-11 sccm. The 15 Volt MKS PR4000-F2V1N power supply was used to provide voltage control to the MFC. The MFC flow rate was varied to minimize errors due to the time delay from the MFC reaching the desired flow rate and minimize the filling time. Lastly, the chamber was vented of ammonia by removing its lid and allowing the fume hood to remove the gas. The experiment set up using a mass flow controller ensures the accuracy in determining the amount of gasses present in the chamber. Previous publications<sup>40-41, 58-62</sup> relied on the

pressure gauge to determine the pressure that was then translated into ppm. The reported method had great uncertainty in determining the amount of gasses present in the testing chamber.

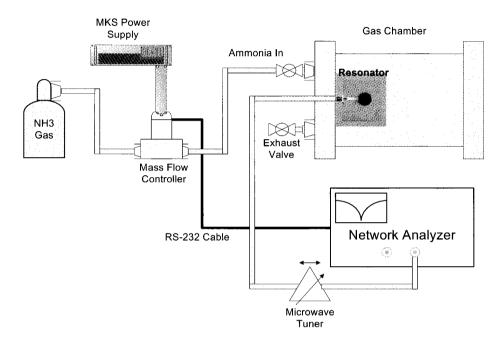


Figure 5. Picture of the experimental set-up

### **4.3 Experimental Results**

The manual impedance tuner was used to match the resonator circuit so that it can achieve a return loss to beyond -40 dB. This low return loss is important in detecting the sensitivity of the resonator sensor. Figure 6 shows the comparison return losses of the 1-port resonator sensor. Upon exposure to ammonia, the resonant frequency shifted to indicate the detection of gasses. When ammonia is removed from the testing chamber, the resonant frequency recovers to its original value. We have also verified that without the carbon nanotube coating, the resonant frequency of the resonator remains unchanged upon exposure to ammonia, at concentrations below 30,000 ppm. Above this concentration, the pressure increase caused by the ammonia is no longer negligible and the center frequency of the resonator decreases with increasing ammonia concentration (increasing pressure). This experiment confirms that the carbon nanotube material enables the sensing capabilities in the microwave resonator. Once we have confirmed that there is a change in the resonant frequency due to the interaction between the ammonia and the carbon nanotubes, we proceeded in conducting experiments to characterize the sensitivity of the microwave resonator sensor.

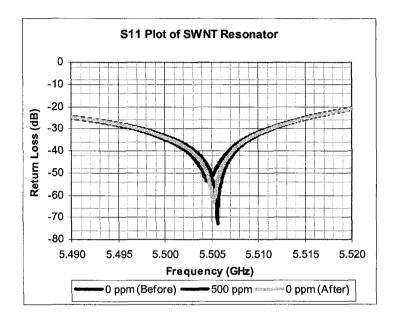
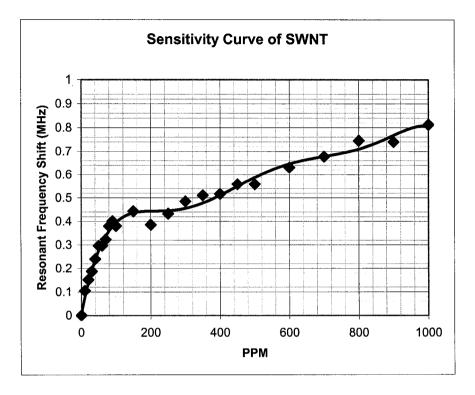


Figure 6. Return losses of the microwave carbon nanotube resonator sensor

To measure the sensitivity, we determined the shift of resonant frequency with respect to the amount of ammonia in the testing chamber. The amount of ammonia flown into the chamber was controlled by a Labview program that allows the response to stabilize. The S-parameters were constantly taken after the response time and a few minutes later. The amount of resonant frequency shift was monitored to be consistent and plotted in Figures 7 and 8. These two figures provide small ppm to demonstrate the working range of the sensor. As seen from Figure 8, the sensitivity of the sensor is very high, up to 4000 Hz/ppm at 100ppm. This is in the order of 1000 times higher than SAW sensor. In addition, the large frequency shift is important in system development to reduce false alarm of the sensor. As the amount of ammonia increases, the sensor still has sensitivity up to 30,000ppm. We stopped the experiment 30,000 ppm, for these concentrations cause the pressure of the chamber to increase to the extent that it begins to lower the resonant frequency of the sensor. It is more important to achieve high sensitivity at low amount of gasses for sensor applications.



Beyond 400ppm, the sensitivity decreases down to 1000 Hz/ppm as shown in Figure 8.

Figure 7. Measured resonant frequency shift versus amount of ammonia at ~5.5 GHz.

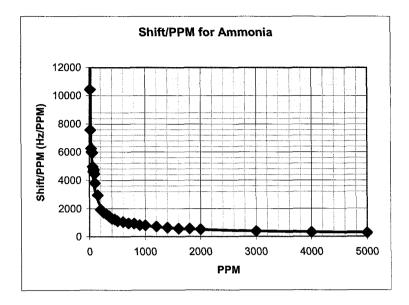


Figure 8. Measured sensitivity (Hz/ppm) of the microwave carbon nanotube resonator sensor at ~5.5 GHz .

Simulations were performed to estimate the effect of the permittivity of the nanotube layer on the resonant frequency. The estimate was obtained by performing simulations with Sonnet<sup>®</sup> and CST<sup>®</sup>. Numerous values for the permittivity of the nanotube cover were used, and it was found that for a permittivity of the cover around 5, the approximate average permittivity of the nanotubes, a change in resonant frequency around 1MHz corresponds to a change in the relative permittivity of 0.15. This change was also found to be approximately linear for frequency changes of a few MHz.

Figure 9 shows the response of the sensor as it is alternately cycled between 10,000 ppm and 0ppm ammonia in an ambient environment. Ammonia was introduced into the chamber as described previously, and the sensor response was allowed to settle. After the response had stabilized, ammonia was removed from the chamber by simply removing its lid and allowing the fume hood to evacuate the ammonia. As seen from the plot, the sensor shows a reversible change in the resonant frequency. It is noted that the value of resonant frequency at 10,000 ppm does not increase after several cycles of dry air and ammonia. This result indicates that the resonant frequency shift is highly repeatable and reversible. This translates into a reversible change in the effective dielectric constant of the resonator sensor. It is noted that this plot cannot be used to estimate the response and recovery time since the time it takes to cycle the gas is quite long for this particular testing chamber. It is assumed that the polar ammonia molecules adhere to the sides of the chamber during the response part

of the test, causing the actual concentration to be slightly lower than expected, and these molecules release during the recovery portion of the test, causing observed response time to be longer than the actual response time. However, the results do demonstrate high degree of repeatability.

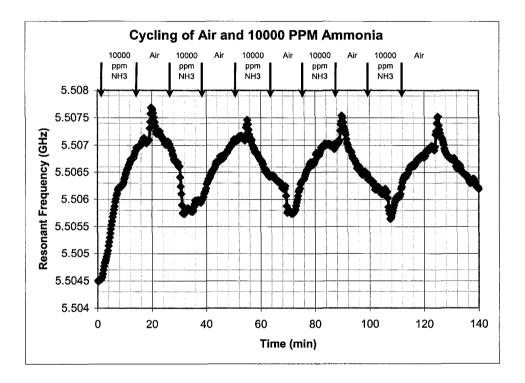
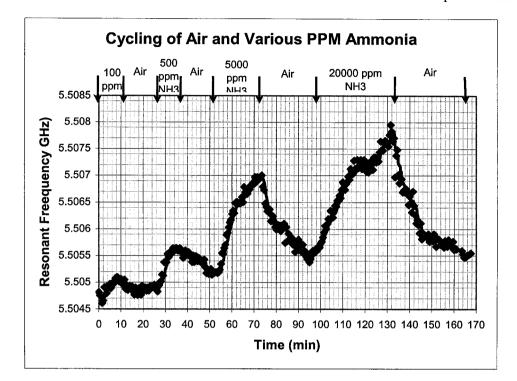


Figure 9. Measured resonant frequency shift when the sensor is cyled between pure ammonia and dry air at 10,000 ppm. The changes are reversible.

Figure 10 shows the response of the sensor as it is alternately cycled between increasing ammonia concentrations and zero concentration in an ambient environment, with an initial ammonia concentration of 100 ppm. The cycling was performed in the same manner as the previous experiment. The results indicate for increasing ammonia cycled with ambient air, the sensor resonant frequency is reversible and its resonant frequency rises with an increase in the ammonia concentration present in the chamber. The sensor can detect



different amount of ammonia with distinct shift and is reversible at different exposure dose.

Figure 10. Measured resonant frequency shift when the sensor is cyled between increasing ammonia concentrations and dry air.

#### 4.4 Sensing Mechanism

Certain gas species have been shown to bind to the nanotubes<sup>38-41, 44-51, 54-56, 58-63</sup>. These gases tend to be oxidizing/reducing agents and also tend transfer charge to the nanotubes. There have been attempts to explain the permittivity change in terms of viewing the absorbed ammonia as having a dielectric constant close to that of its liquid state, 22. Since the dielectric constant of the nanotubes is around 5, it has been proposed that the effect of the absorbed ammonia is to raise the dielectric constant of the nanotube layer by means of an averaging process. However, we have observed an increase in the resonant frequency, which implies that the permittivity of the nanotube cover is decreasing. We have also observed that coating the resonant frequency upon exposure to ammonia. Assuming the dielectric constant of the multiwalled nanotubes is of the same order of the individual Single walled nanotubes, this observation implies another mechanism for the change of the dielectric constant. The results do correlate with the oxidizing/ reducing nature of the gas and the state

of the nanotube coating. Ammonia, a reducing agent, donates electrons to the nanotube $^{72}$ . Since the single walled nanotube coating is p-type due to the effect of defects<sup>38, 41</sup>, the donated electrons tend to cancel out the holes and thus reduce the conductivity. The vertically grown array of Multi-walled nanotubes yields relatively pristine, defect free, tubes. Since oxygenation has been shown to occur at the defect sites<sup>41</sup>, the lack of defect sites indicates the tubes should be virtually intrinsic, so donated electrons increase the conductivity and permittivity. This change in conductivity manifest it self in a change in permittivity. The imaginary part and real parts of the permittivity increase monotonically with conductivity. In reference 73, the permittivity of metallic nanotubes was found to increase proportionally to the square of the Fermi level, with a positive additive term reflecting the increase of carrier concentration with temperature. The results here suggest that for our nanotube coating, consisting of tubes with a wide range of properties, that the carrier density is the dominant factor. Although it may seem counterintuitive that conductivity affects the real part of the permittivity, the Kramers-Kronig relations suggest that in order for the permittivity to be a real, causal function, the imaginary and real parts are related. If the effect of the added charge was to simply increase the conductivity over the entire frequency range or to only increase the low frequency conductivity, the transformations suggest the results presented here. However, detailed data on the frequency dependence of the conductivity is unavailable, and the exact relationship between the change in conductivity and the real part of the permittivity has yet to be determined. That relationship may also serve to explain the small percentage change of resonant frequency in this resonant sensor compared to the order of magnitude change of DC conductivity in conductivity sensors. In summary, the effect of an increase in conductivity results in an increase of loss, a decrease in Q, an increase in the effective dielectric constant, and an decrease in the resonant frequency. A decrease in conductivity should cause the opposite effect.

#### V. Wireless Sensing Efforts

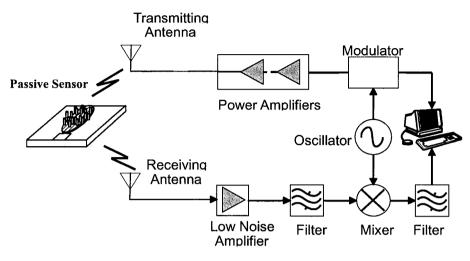


Figure 11. Illustration of wireless sensor system.

Wireless sensors have been implemented in various ways. Two main categories of the passive variety are continuous and pulsed interrogation. Pulsed interrogation involves switching the interrogation single on and off. The signal would interact with the sensor and be reflected back. When this signal reaches the receiver, the interrogating signal will be The received signal would be that of the original signal, but it will have turned off. undergone amplitude and phase variations. These variations will contain the information to be monitored. Demonstrations have used FM signals to interrogate the sensor in this pulsed manner, by mixing the interrogating signal with the received signal and using the output(containing information of the phase shift) to quantify the parameter to be sensed. Varadan has used an additional antenna on the sensor to serve as reference to eliminate the interference caused by the differences in sensor location from the interrogator. Another approach is to use two SAW resonators, with one used as a reference. The output signal is the difference in delays of the two, and this helps to greatly reduce the sensitivities to the RF channel<sup>84</sup>. These methods are limited to high Q sensing devices. Devices must be able to store energy for relatively long periods of time, thus decreasing the switching speeds required for transmitter/receiver system. SAW are capable of this kind of interrogation $^{74}$ . Spectral domain sensors are not suited for pulsed interrogation in a cost efficient manner. The required switching times are very short.

The other type of interrogation is characterized by a continuous interrogating signal. Kong et al have demonstrated this with carbon nanotube coated LC-tank sensor by monitoring the impedance of a loop antenna in the vicinity of the sensor with an impedance analyzer<sup>56</sup>. Similar results have been obtained by Yoon, with FM modulation of the interrogating signal<sup>55</sup>. Although this has been shown to work, it is very sensitive on the location of the sensor, as well as environmental factors affecting the RF channel. The ideal situation would be to modulate the information onto the carrier signal at the sensor itself.

## VI. Carbon Nanotube Functionalization Efforts

Although nanotubes have been shown here to be significantly sensitive to Ammonia, as well as NO<sub>2</sub> and other toxic substances elsewhere, many substances that are of interest do not react significantly with the intrinsic nanotubes. Also, it is desirable to increase sensitivity, selectivity, increase response time, and decrease recovery time. Nanotubes have been functionalized by various means to address these issues for different applications<sup>75-83</sup>. Nanotubes doped with nitrogen (CN<sub>x</sub> tubes) have been used in conductivity sensors and have shown responses to relatively high concentrations (>1%) of ammonia, acetone, ethanol, and chloroform<sup>75</sup> Nanotubes gasoline, pyridine. have been doped with poly-m-aminobenzene sulfonic acid for use in a conductivity sensor, resulting in a reported two-fold increase in sensitivity to ammonia<sup>77</sup>. Tin Oxide coatings of 1-6nm have also been reported for nanotubes<sup>76, 78</sup>. Sensors have been constructed with these structures with responses for ppm concentrations of NO, NO<sub>2</sub>, ethanal, and C<sub>2</sub>H<sub>2</sub>. Nanotubes have been used in conjuction with a Pd thin film for hydrogen detection with some success<sup>79</sup>. Doping nanotubes with Pd has been demonstrated to be very effective, with sensitivities to .5% H<sub>2</sub> in a nitrogen environment<sup>80</sup>. However, these tin oxide and palladium functionalized sensors do require temperatures in excess of 200  $C^0$ . Amidoferrocenyl-functionalized nanotubes have been demonstrated to recognize the presence of mM concentrations of  $H_2PO_4$ - at room temperature<sup>83</sup>. Room temperature responses have been observed for 6ppm of methanol with Pd loaded carbon nanotubes<sup>69</sup>. Peng and Cho have shown the possible detection of CO with carbon nanotubes doped with boron and nitrogen, and they have also suggested that sensitivity can be controlled through doping<sup>68</sup>. Further research is needed to see if other molecules could be used to aid selective reactivity at room temperature and ambient conditions. It has been shown that the charge transfer to nanotubes depends on their chirality, and that metallic tubes have the fastest rate of charge transfer. It was also shown that the smallest band gap

tubes have a tenfold increase in their charge transfer rate, implying the ability to tune response/recovery times<sup>84</sup>. Although constructing a layer of tubes of a single chirality is a daunting task, chiral selective charge transfer offers hope in improving our ability to select tubes of specific properties in the future.

### VII. Future Research

Our research efforts are focused on developing a robust wireless sensor node with tunable selectivity. Wireless sensing has been demonstrated, but there is still progress to be made in reliability and cost reduction. Our current research regarding the wireless aspect of this project involves reducing the sensitivity of the wireless node to its environment, while increasing its sensitivity with respect to the species to be detected. The main challenge for the wireless aspect of the node is the sensitivity of the RF channel to the surrounding environment and the dependence of the measurand to the RF channel. Also, we are investigating ways in which to make the carbon nanotubes a suitable transducer for a wider range of species through fictionalization and increasing its selectivity either through fictionalization or mass selective polymer coatings.

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# ELECTROSTATICS OF NANOWIRES AND NANOTUBES: APPLICATION FOR FIELD-EFFECT DEVICES

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We present a quantum and classical theory of electronic devices with one-dimensional (1D) channels made of a single carbon nanotube or a semiconductor nanowire. An essential component of the device theory is a self-consistent model for electrostatics of 1D systems. It is demonstrated that specific screening properties of 1D wires result in a charge distribution in the channel different from that in bulk devices. The drift-diffusion model has been applied for studying transport in a long channel 1D field-effect transistor. A unified self-consistent description is given for both a semiconductor nanowire and a single-wall nanotube. Within this basic model we analytically calculate equilibrium (at zero current) and quasi-equilibrium (at small current) charge distributions in the channel. Numerical results are presented for arbitrary values of the driving current. General analytic expressions, found for basic device characteristic, differ from equations for a standard bulk three-dimensional field-effect device. The device characteristics are shown to be sensitive to the gate and leads geometry and are analyzed separately for bulk, planar and quasi-1D contacts. The basic model is generalized to take into account external charges which can be polarized and/or moving near the channel. These charges change the self-consistent potential profile in the channel and may show up in device properties, for instance, a hysteresis may develop which can have a memory application.

*Keywords*: electrostatics of low-dimensional systems; device physics; nanotube and nanowire transistors.

## 1. Introduction

A basic trend in modern electronics is the wider device application of nanostructures, having at least one geometric size a less than some characteristic electron length: de Broglie wavelength  $\lambda$ , electron mean free path  $l_{tr}$ , or Debye screening radius  $r_s$ . For  $a \sim \lambda$  the electronic properties of nanostructures are strongly modified by size quantization of the energy spectrum, while for  $a < l_{tr}$  transport acquires ballistic character. Influence of these two phenomena on the characteristics of various low-dimensional devices has been widely discussed in the literature. In the present paper, partially based on our short communication <sup>1</sup>, we consider modification of the screening phenomena in nanowires and nanotubes with the radius *a* less than  $r_s$  and apply this knowledge to the problem of a field-effect transistor (FET) based on these quasi-one-dimensional (quasi-1D) nanostructures.

All low-dimensional systems are characterized by dramatic suppression of electron screening as compared to bulk semiconductors. Therefore, a different theoretical approach has to be used for the calculation of a screened potential  $\phi$ . In bulk materials,  $\phi(\mathbf{r})$  is found from the Poisson equation where the induced charge is proportional to the Laplacian (second derivative) of  $\phi$ . In low-dimensional systems, for determination of  $\phi(\mathbf{r})$  one should solve the Laplace, rather than Poisson, equation containing the screening charge in boundary conditions. For two-dimensional electrons (see, e.g., <sup>2</sup>) the surface charge density is proportional to the field, the first derivative of potential. Similar dimensional analysis for quasi-1D nanowires <sup>3</sup> shows that for slow charge and potential variations (with the characteristic length  $l \gg a$ ), the one-dimensional charge density  $\eta(x)$  is simply proportional to local value of an induced potential at the nanowire surface:

$$\phi^{ind}(x,a) \simeq \frac{2}{\varepsilon} \ln\left(\frac{l}{a}\right) \eta(x)$$
 (1)

where  $\varepsilon$  is the dielectric constant of the medium outside nanowire. The weak screening in 1D case is due to the fact that any charge in a system creates electric field in the whole environment, including both the wire and the surrounding medium, while the carriers responsible for screening are severely restricted in their motion to one single direction along the wire. This differs drastically from bulk semiconductors with carriers present in all points where electric field exists and providing effective screening by re-distributing in this field.

On the basis of Eq.(1) a self-consistent electrostatics of quasi-1D systems can be easily formulated and used for modelling of a number of 1D applications, including transport and memory devices  $^{1,4}$ , optics  $^5$ , nanoelectromechanical systems  $^6$ , and even artificial ion channels  $^7$ . In the present paper we restrict ourselves to electronics applications.

The paper proceeds as follows. Sec.2 presents the basic equations to be solved to calculate the charge density and current in 1D FET. Sec.3 gives a solution of these equations for the case of bulk electrodes. We show in Sec.4 that an analytical treatment of the model is possible at low drain voltage. The next section presents numerical results for an arbitrary drain voltage, that are given separately for Ohmic and injecting contacts in Sec.5.1 and 5.2 respectively. In this part of the paper we closely follow our earlier results (published in <sup>1,4</sup>), which review is needed to emphasize on the role of the contact geometry in last two sections. Though, it follows from the general expressions of Sec.2 that the potential profile along the channel is a function of the contact geometry, in this paper we add new evidence for this. Sec.6 deals with the cases of 2D and 1D contacts, presenting for the first time analytical expressions for equilibrium charge distribution and, thus, transconductance of the 1D FET. Last section reviews the role of the charge injected into the substrate and gives a description for the hysteresis in a real 1D FET structure.

## 2. Formulation of the problem: Device geometry

We consider a 1D FET in which the channel is a semiconductor nanowire or a carbon nanotube. The schematic geometry of such FET is shown in Fig.1. The structure includes the source (x < -L/2) and drain (x > L/2) electrodes (in our model they are assumed to be identical) connected by a nanowire of the length L. The gate electrode is separated by a thin dielectric layer of the thickness d. We assume the wire to be uniformly doped with the linear concentration N = const(x) (in pristine nanotubes N = 0). In the absence of source-drain voltage the equilibrium carrier concentration in the channel has some symmetric profile  $n_0(x)$ , which may differ from N and be coordinate-dependent. This profile is due to the contact potentials between the channel and electrodes determined by their work function difference, any electric potential induced by charges in the environment (in particular, movable charges), and the gate voltage  $V_q$ . When the structure is in operation, the sourcedrain voltage  $V_d$  causes a current j along the channel and thus a re-distribution of carrier concentration as compared with  $n_0(x)$ . The voltage  $V_g$  (and also the potential of the variable charge in the environment, which is presented in the case of a nanotube nonvolatile memory, for example  $^{26,27,28}$ ) changes the concentration in a channel controlling the FET transport. We employ the drift-diffusion model in this paper and assume that the scattering rate in the channel is sufficiently high to support a local charge equilibrium assumption. This is likely valid for the most of the nanowire FETs and, at least, for some of nanotube devices. In the opposite (ballistic) limit, discussed in <sup>8</sup>, the channel and contact geometry influences the device characteristics via lowering the tunnel barriers at the source and/or drain. Nevertheless, the device electrostatics is one of the most important factors for the total conductance. In this work we restrict ourselves to the case of drift-diffusion transport when the modulation of the channel conductance is determinant for the transport through the whole device.

We measure all potentials from the middle point of the wire (x = 0) so that the source and drain potentials are  $-V_d/2$  and  $V_d/2$ . In this case the potentials along the wire and concentration changes caused by  $V_g$  together with the contact potentials and by  $V_d$  are, respectively, symmetric and antisymmetric functions of xand will be denoted by the subscripts s and a:  $\phi_{s,a}(x)$  and  $n_{s,a}(x)$ . The potential of any external charges, movable or not, has no specific symmetry. This is a random function of x and has to be averaged over the distribution of the charge centers (a possible averaging procedure for 2D charge impurities can be found in <sup>9</sup>). Since the movable charges in the environment obey the same electrostatics as the movable charges in the tube, it is rational to assume that their potential, on average, will

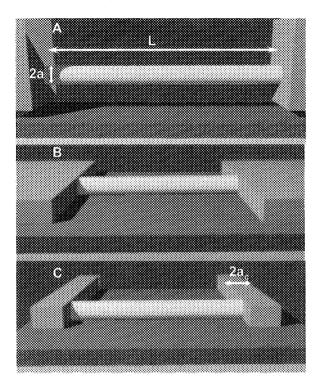


Figure 1: Possible geometry of contacts to a 1D FET: (A) 3D contacts (all dimensions are much larger than the channel width), (B) 2D contacts and (C) 1D contacts. The potential profile along the weakly screening 1D channel depends on the dimension (and other geometry) of the contacts, which results in a different device behavior.

have also a similar coordinate dependence as the total electrostatic potential. For the sake of clarity, in the most part of the paper, except for Sec.7, no external movable/polarizable charge will be considered.

The potentials  $\phi_{s,a}(x)$  can be divided into two parts: the components  $\phi_{s,a}^0(x)$  created by electrodes and contact potentials, which should be found from the Laplace equation containing no wire charge, and the components  $\phi_{s,a}^1(x)$  caused by the electron charge in a wire  $-en_{s,a}(x)$ . We assume that the characteristic lengths L and d determining the potential and concentration distribution along the wire, exceed noticeably the wire radius a. In this case the relationship between  $\phi_{s,a}^1(x)$  and  $\rho(x)$  is given by the linear formula Eq.(1). Using this relationship, the current j containing both drift and diffusion components\*can be written for a semiconductor nanowire

<sup>\*</sup>Contrary to three- and two-dimensional electron systems where the role of diffusion current at the distances much larger than the screening length is negligible, in quasi-one-dimensional electron systems its contribution is parametrically the same as that of drift current caused by  $\phi^1$  and cannot be ignored.

with non-degenerate carriers in the form  $^{10}$ :

$$\frac{j}{e\mu} = n(x)\frac{d\phi^0}{dx} - \left[\frac{2e}{\varepsilon}\ln\left(\frac{l}{a}\right)n(x) + \frac{kT}{e}\right]\frac{dn}{dx}$$
(2)

where  $n = n_s + n_a$ ,  $\phi^0 = \phi_s^0 + \phi_a^0$ ,  $\mu$  is the carrier mobility, and the characteristic length of charge variation along the wire *l* in our case has the order of min{L, 2d}. For a nanotube with N = 0 and degenerate carriers, kT should be replaced by the concentration-dependent Fermi energy and, instead of Eq.(2), we have <sup>11,12</sup>:

$$\frac{j}{e\mu} = n(x)\frac{d\phi^0}{dx} - eC_t^{-1}n(x)\frac{dn}{dx},\tag{3}$$

where  $C_t^{-1}$  is the inverse capacitance of the nanotube derived in <sup>11</sup> and containing both logarithmic geometrical capacitance similar to Eq.(2) and the quantum capacitance of the 1D electron gas,  $1/(e^2\nu) \simeq 0.31$  for one degenerate subband of a single wall nanotube with the density of states  $\nu$ .

Eq.(3) is easier to solve than Eq.(2) and in this connection it is important to note that at some conditions the latter can be also reduced to a simpler form. It can be easily shown that at  $A \equiv (2e^2N/\varepsilon kT)\ln(l/a) \gg 1$  the last term in Eq.(2) can be neglected and it acquires the form of Eq.(3) with  $C_t^{-1} = (2/\varepsilon)\ln(l/a)$ . This has a rather simple explanation. Two terms in the square brackets in Eq.(2) correspond, respectively, to drift in a self-consistent electric field and to diffusion. In degenerate nanotubes these terms have exactly the same appearance and may be written as a single term with the coefficient  $C_t^{-1}$ . In a non-degenerate system the terms are different but for  $A \gg 1$  the diffusion term can be neglected.

We will solve the first order differential equation for n(x) given by Eq.(2) or (3), with the boundary conditions

$$n(\pm L/2) = n_c \tag{4}$$

assuming the source and drain to support constant concentration at the contacts, independent of the applied voltage. The two conditions Eq.(4) allow us to determine the integration constant and the value of current j so far considered as some unknown constant.

Depending on the relationship between  $n_c$  and N, three possible situations can be realized. The condition  $n_c = N$  corresponds to ideal Ohmic contacts not disturbing electric properties of a wire,  $n_c > N$  describes the situation where the carriers are provided by electrodes, which is often the case for nanotubes, and  $n_c < N$ corresponds to depleted Schottky contacts. In the latter case, the regions near contacts have the lowest carrier concentration and determine the current through the structure. At the same time, this concentration is fixed by Eq.(4) and does not depend on  $V_g$ . As a result, for the structures adequately described by the classical drift-diffusion theory (see Eq.(2)), transconductance will be very small. The only possible situation of an applied interest is that when the Schottky barrier has a noticeable tunnel transparency strongly dependent on  $V_g$ . This situation has been thoroughly considered in <sup>8,13</sup> and will not be discussed below.

#### 3. Potential profile: 3D bulk electrodes

The first step in calculating characteristics of a particular FET consists in finding the potential profile  $\phi^0(x)$  along the channel. For  $n_c = N$  it can be done by direct solution of the Laplace equation determining the potential  $\Phi(x, y)$  created by the given system of electrodes<sup>†</sup> However, for  $n_c \neq N$  the basic formulae of the previous section require some modification. In the closest vicinity of contacts there exists a finite charge density  $e(N-n_c)$  in a wire. To provide equipotentiality of metallic contacts, we must assume the presence of charges of the opposite sign (image charges) just beyond the contacts. This means discontinuity of charge density at  $x = \pm L/2$ and makes doubtful the adequacy of Eq.(1) assuming smooth charge and potential variations. To avoid this difficulty, we will measure n from  $n_c$  by assuming in Eq.(2)  $n(x) = n_c + \Delta n(x)$ . In this case, the boundary conditions Eq.(4) are replaced by

$$\Delta n(\pm L/2) = 0 \tag{5}$$

but the potential acquires an additional term  $\phi_c(x)$ :

$$\phi_s^0(x) = \phi_c(x) + \phi_g(x) \tag{6}$$

where  $\phi_g(x)$ , as earlier, is determined by the gate, source and drain electrodes at  $V_d = 0$  while  $\phi_c(x)$  is a potential of a wire with uniform charge  $e(N - n_c)$  between metallic contacts at  $x = \pm L/2$ . This is just the charge which, together with its images, may have discontinuities at the contacts.

In this section we calculate  $\phi^0(x)$  for the case of bulk contacts representing metallic or heavily doped semiconductor regions with all three dimensions considerably exceeding the characteristic lengths a, d and L. In this case the contact size can be assumed infinite as it is shown in Fig.1A. Exact calculations are rather cumbersome and to obtain relatively simple analytical results, we make some additional approximation. Let us assume that the relation  $d \ll L$ , often realized in 1D FETs, is fulfilled in our system as well. In this case the potential distribution in the most part of inter-electrode space will not noticeably change if we neglect the dielectricfilled slit of the thickness d between the channel and the gate. In other words, we solve the Laplace equation  $\Delta \Phi = 0$  in the semi-infinite strip -L/2 < x < L/2; y > 0 with the boundary conditions:  $\Phi(y = 0) = V_g$ ;  $\Phi(x = \pm L/2) = \pm V_d/2$  and then, assuming y = d and adding the expression for  $\phi_c(x)$  derived in <sup>10</sup>, obtain the following formulae for  $\phi_{s,a}^0(x)$ :

<sup>&</sup>lt;sup>†</sup>Here and henceforth  $\Phi(x, y)$  represents the complete solution of the Laplace equation whereas  $\phi(x) \equiv \Phi(x, d)$  is the potential along the wire.

$$\begin{split} \phi_s^0(x) &= \phi_c(x) + \phi_g(x) = \frac{8e(N-n_c)L}{\pi^2 \varepsilon a} \\ &\times \sum_{n=0}^\infty \frac{(-1)^n}{(2n+1)^2} \frac{\left\{ K_0 \left[ \frac{\pi a}{L} (2n+1) \right] - K_0 \left[ \frac{2\pi d}{L} (2n+1) \right] \right\}}{K_1 \left[ \frac{\pi a}{L} (2n+1) \right]} \cos\left[ \frac{\pi x (2n+1)}{L} \right] \end{split}$$

$$+\frac{4V_g}{\pi}\sum_{n=0}^{\infty}\frac{(-1)^n}{(2n+1)}\cos\left[\frac{\pi x(2n+1)}{L}\right]\exp\left[-\frac{\pi d(2n+1)}{L}\right];$$
(7)

$$\phi_a^0(x) = V_d \left[ \frac{x}{L} + \sum_{n=1}^{\infty} \frac{(-1)^n}{\pi n} \sin\left(\frac{2\pi xn}{L}\right) \exp\left(-\frac{2\pi dn}{L}\right) \right]$$
(8)

where  $K_0$  and  $K_1$  are Bessel functions of an imaginary argument <sup>14</sup>.

### 4. Linear conductivity and transconductance

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Now we can calculate the carrier concentration  $\Delta n$  and the electric current j caused by the driving voltage  $V_d$ . The problem is relatively simple if we restrict ourselves to the linear case by assuming  $V_d$  to be sufficiently small. In the zeroth approximation j = 0 and both  $\phi^0(x)$  and n(x) contain only a symmetric component and are the same as in equilibrium:  $\phi_s^0(x) = \phi_c(x) + \phi_g(x)$ ,  $n_s(x) = n_c + \Delta n_0(x)$  where the equation for  $\Delta n_0(x)$  is:

$$[n_c + \Delta n_0(x)] \frac{d\phi_s^0}{dx} - \left\{ \frac{2e}{\varepsilon} \ln\left(\frac{l}{a}\right) [n_c + \Delta n_0(x)] + \frac{kT}{e} \right\} \frac{d(\Delta n_0)}{dx} = 0.$$
(9)

Direct integration of Eq.(9) with the boundary conditions Eq.(5) transforms it into an algebraic equation for  $\Delta n_0$ :

$$\ln\left(1 + \frac{\Delta n_0(x)}{n_c}\right) + \frac{2e^2}{\varepsilon kT} \ln\left(\frac{l}{a}\right) \Delta n_0(x) = \frac{e\phi_s^0(x)}{kT}.$$
 (10)

For degenerate carriers in a nanotube (or for  $A \gg 1$ ), the problem is much simpler since, according to Eq.(3),  $\Delta n_0(x)$  is proportional to  $\phi_s^0(x)$ :

$$\Delta n_0(x) = C_t \phi_s^0(x). \tag{11}$$

We emphasize that Eqs.(2),(3) were derived in the drift-diffusion approximation. On the contrary, the expressions of this section, being equilibrium, remain adequate beyond the drift-diffusion model.

To the first order in  $V_d$ , the differential equations (2),(3) can be linearized in  $n_a$ . The equation for a nanowire reads as:

$$\left[\frac{2e}{\varepsilon}\ln\left(\frac{l}{a}\right)\left[n_{c}+\Delta n_{0}(x)\right]+\frac{kT}{e}\right]\frac{dn_{a}}{dx}+\left[\frac{2e}{\varepsilon}\ln\left(\frac{l}{a}\right)\frac{d(\Delta n_{0})}{dx}-\frac{d\phi_{s}^{0}}{dx}\right]n_{a}(x)$$

$$=\left[n_{c}+\Delta n_{0}(x)\right]\frac{d\phi_{a}^{0}}{dx}-\frac{j}{e\mu}.$$
(12)

Since  $\phi_a^0(x)$  is proportional to  $V_d$ , both  $n_a(x)$  and j are also linear in  $V_d$ . Eq.(12), being solved with the conditions  $n_a(0) = n_a(L/2) = 0$ , gives the current-induced change of concentration profile  $n_a(x)$  and the implicit expression for the current j:

$$\int_{0}^{L/2} \exp\left[\int_{0}^{x} \frac{\left[\frac{2e}{\varepsilon}\ln\left(\frac{l}{a}\right)\frac{d(\Delta n_{0})}{dx'} - \frac{d\phi_{a}^{0}}{dx'}\right]dx'}{\frac{2e}{\varepsilon}\ln\left(\frac{l}{a}\right)\left[n_{c} + \Delta n_{0}(x')\right] + \frac{kT}{e}}\right] \frac{\left[\left[n_{c} + \Delta n_{0}(x)\right]\frac{d\phi_{a}^{0}}{dx} - \frac{j}{e\mu}\right]dx}{\frac{2e}{\varepsilon}\ln\left(\frac{l}{a}\right)\left[n_{c} + \Delta n_{0}(x)\right] + \frac{kT}{e}} = 0.$$
(13)

The resulting j depends on the gate voltage  $V_g$  through the functions  $\phi_s^0(x)$  and  $\Delta n_0(x)$ , which allows us to calculate the transistor transconductance  $s = dj/dV_g$ .

For  $A \gg 1$  the problem is essentially simplified and, as it has been already mentioned, this case coincides with that for a degenerate nanotube. Instead of Eq.(12), we have:

$$C_t^{-1}[n_c + \Delta n_0(x)]\frac{dn_a}{dx} = [n_c + \Delta n_0(x)]\frac{d\phi_a^0}{dx} - \frac{j}{e\mu}$$
(14)

which gives us directly

$$n_a(x) = C_t \left\{ \phi_a^0(x) + \frac{V_d}{2} - \frac{j}{e\mu} \int_{-L/2}^x \frac{dx'}{[n_c + \Delta n_a(x')]} \right\}$$
(15)

where

$$j = \frac{V_d}{R}, \qquad R = \frac{2}{e\mu} \int_0^{L/2} \frac{dx}{[n_c + \Delta n_0(x)]}.$$
 (16)

The last expression is the ordinary Kirchhoff's law, which is not surprising since the condition  $A \gg 1$  is equivalent to neglection the diffusion component of current. Taking into account Eq.(11), we can re-write the last expression in terms of the dimensionless channel conductance  $\sigma = jL/(n_c e \mu V_d)$ :

$$\sigma = \left[2\int_{0}^{1/2} \frac{dt}{1+g\Psi(t)}\right]^{-1}$$
(17)

where

$$g = \frac{2\varepsilon V_g}{\pi e n_c \ln\left(l/a\right)} \tag{18}$$

and for  $n_c = N$ ,

$$\Psi(t) = \sum_{0}^{\infty} \frac{(-1)^n}{(2n+1)} \cos[\pi t(2n+1)] \exp[-\frac{\pi d(2n+1)}{L}].$$
 (19)

The  $\sigma(g)$  dependence has a cut-off voltage  $g_0 = -\Psi^{-1}(0)$  characterized by vanishing  $\sigma$  and strong increase of  $d\sigma/dg$  to the right of  $g_0$ . The exact behavior of these characteristics near the cut-off can be calculated analytically. They are determined by the point of minimal equilibrium concentration, which in a symmetric structure is x = 0, and hence by the properties of  $\Psi(t)$  at small t. It can be easily shown that in this region  $\Psi(t) \simeq \pi/2 - \arctan[\exp(-\pi d/L)] - (\pi^2 t^2/2) \sinh(\pi d/L)/\cosh^2(\pi d/L)$ , which allows us to perform integration in Eq.(17) and obtain

$$\sigma = \frac{\sqrt{(g - g_0) \sinh(\pi d/L)}}{\sqrt{2} \cosh(\pi d/L)},$$

$$g_0 = -\frac{1}{\pi/2 - \arctan[\exp(\pi d/L)]}.$$
(20)

Thus the transconductance  $s = d\sigma/dg$  diverges at the cut-off  $\sim (g - g_0)^{-1/2}$ .

If  $n_c \neq N$ , the result given by Eq.(20) will not change qualitatively. In this case the function  $\Psi(t)$  contains additional contribution from  $\phi_c(x)$ . This function, studied in more detail in <sup>10</sup>, behaves non-analytically at  $x \to \pm L/2$  but, similarly to  $\phi_g(x)$ , has an extremum at x = 0 and can be expanded in this point. This modifies the value of  $g_0$  and the coefficient in *i* but retains unchanged the square-root character of  $\sigma(g)$  and the divergence of *s*.

The simplified expressions Eqs.(11),(14),(16),(17) neglected diffusion effects, which is equivalent to the limit of zero temperature. The resulting carrier distribution Eq.(11) does not take into account activation processes and simply gives  $n_s = 0$  for all points where  $\phi_s^0(x) < -C_t^{-1}n_c$ . The potential  $\phi_s^0$  and the carrier concentration acquire their minimal values at x = 0 and, hence, in the linear approximation, the cut-off voltage  $g_0$  corresponds to the condition  $\phi_s^0(0) = -C_t^{-1}n_c$  and at lower g the current is exactly zero. At non-zero temperatures the current at  $q < q_0$  will have an activation character because of thermal tails of the carrier distribution function:  $j \sim \exp(-\Delta/kT)$  where  $\Delta = e\left(-C_t^{-1}n_c - \phi_s^0(0)\right)$  is the barrier height. Since  $\phi_s^0(0)$ depends linearly on  $V_g$  (see, for instance, Eq.(7)), the activation energy  $\Delta$  is directly proportional to  $g_0 - g$ . This means, in turn, that the above-mentioned singularity of  $d\sigma/dg$  is fictitious. In fact, its g-dependence will have some maximum at  $g_0$  with a sharp, temperature-dependent decrease at lower q. We do not consider here a tunnelling, though this effect may be important, especially if the carrier effective mass is small, as in the case of a single-wall nanotube. The tunnelling is easily included in a Wentzel-Kramers-Brilloin approximation <sup>15</sup> (details of the calculation for single-wall nanotubes can be found elsewhere  $^{16}$ ).

#### 5. Current–voltage characteristic of the channel

So far we have dealt with the linear channel conductivity and transconductance at a low source-drain voltage  $V_d$ . Another important FET characteristic — the channel current-voltage characteristic (IVC) — and its dependence on the gate voltage and the temperature, can be obtained only by a numerical solution of the Eqs.(2),(3). It is convenient to use dimensionless variables measuring concentrations in units of  $n_c$ , lengths in units of L, potentials in units of  $en_c/\varepsilon$  and current in units of  $e^2n_c^2\mu/(L\varepsilon)$ . The new dimensionless gate potential is related to the parameter g introduced in 946 A. Shik, H. E. Ruda & S. V. Rotkin

Sec.4 as  $V_g = (\pi g/2) \ln (l/a)$ . For these dimensionless units the basic equation (2) acquires the form

$$j = n(x)\frac{d\phi}{dx} - \left[2\ln\left(\frac{l}{a}\right)n(x) + \tau\right]\frac{dn}{dx}$$
(21)

where  $\tau = \varepsilon kT/(e^2n_c)$  is the dimensionless temperature. The potential consists of three parts:  $\phi(x) = \phi_c(x) + \phi_g(x) + \phi_a(x)$  describing the influence of contact work function, gate voltage and source-drain voltage and proportional to  $N - n_c$ ,  $V_g$  and  $V_d$ , respectively. The particular form of these terms depends on the geometry of contacts and, e.g., for bulk contacts is given by Eqs.(7),(8). The dimensionless version of Eq.(3) for nanotubes can be easily derived from Eq.(21) by assuming  $\tau = 0$  and replacing  $2 \ln (l/a) \rightarrow \varepsilon C_t^{-1}$ .

Eq.(21) should be solved with the two boundary conditions:  $n(\pm 1/2) = 1$ , which determine the integration constant and the so far unknown value of j. Since  $\phi_g(x)$  is proportional to  $V_g$  and  $\phi_a(x)$  is proportional to  $V_d$ , the resulting solution gives us the IVC of a nanowire  $j(V_d)$  for various gate voltages.

For our numerical calculations we choose particular values  $\ln (l/a) = 3$  and d/L = 0.3. Calculations were performed for two situation: ideal Ohmic contacts with  $n_c = N$  and undoped nanowire (nanotube) with injecting contacts: N = 0.

## 5.1. Ohmic contacts

In this case the component  $\phi_c(x)$  in Eq.(7) is absent and the dimensionless threshold voltage  $V_{g0}$ , being estimated with Eq.(20) (that is, in the limit of low temperatures), is equal to -12.8 for our set of parameters. Fig.2 shows IVC at two gate voltages:  $V_q = -13.2$  (below the threshold) and  $V_q = -12$  (above the threshold). All characteristics have a superlinear character, which has a simple explanation. High driving voltage  $V_d$  tends to distribute carriers uniformly along the channel. In our conditions when powerful contact reservoirs fix the concentration n at the points where it is maximal, at the source and the drain, such a re-distribution will increase the minimal value n in the center of channel and hence increase conductivity of the latter. Such superlinear behavior experimentally observed in nanowire-based transistors  $^{17,18,19,20}$  differs noticeably from a sublinear dependence typical for both bulk FETs and ballistic nanotube <sup>21,22,23</sup> structures. We assume that the mechanism of the IVC saturation is due to the contact resistance  $R_c$  not included in our theory. When the channel resistance becomes much less than the contact resistance,  $R \ll R_c$ , almost all the bias drops at the contacts and the current saturates at  $V_d/R_c$ .

Fig.2 presents also information on temperature dependence of the channel conductivity. This dependence is practically absent above the threshold. The IVC curves for  $V_g = -12$  at different temperatures do not deviate more than by 10% from the dashed line corresponding to a fixed temperature  $\tau = 0.2$ , and for this reason are not shown in the figure. For  $V_g$  below the threshold and for not very large  $V_d$ , Fig.2 demonstrates a strong temperature dependence of the current shown

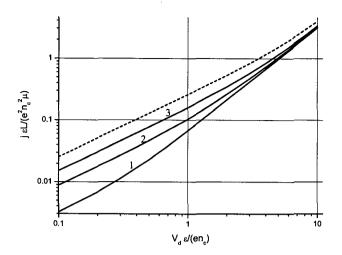


Figure 2: IVC of a 1D FET with d/L = 0.3 and Ohmic contacts at different gate voltages:  $V_g = -12$  (dashed line) and  $V_g = -13.2$  (solid lines) for the temperatures:  $\tau = 0.05$  (1); 0.1 (2), and 0.2 (3). (Curves for all three temperatures and  $V_g = -12$  coincide.)

in more details in Fig.3. The current is calculated for low  $V_d = 0.1$ , corresponding to the initial linear part of the IVC. Two upper curves, corresponding to the above-threshold  $V_g$ , have no noticeable temperature dependence. In contrast, two lower curves demonstrate such a dependence with the activation energy growing with  $|V_g|$ , in accordance with the predictions of Sec.4. At high  $V_d$ , where contact injection and electric field tend to create uniform carrier concentration equal to  $n_c$ , different IVC curves become closer and the temperature dependence collapses.

## 5.2. Injecting contacts

Though this case formally differs from that considered in the previous subsection, it is only due to the presence of a term  $d\phi_c(x)/dx$  in Eq.(21). As it can be seen from Eq.(7), this derivative has singularities at the contacts, which complicates the numerical calculations. To get rid of these singularities, we use the following trick. In the closest vicinity of contacts the first term in the right side of Eq.(21) tends to infinity so that we can neglect the coordinate-independent left side. The remaining terms correspond to a quasi-equilibrium carrier distribution described by Eq.(10) with  $\phi_c$  playing the role of  $\phi_s^0$ . This formula gives the concentration profile in the vicinity of contacts, which allows us to solve Eq.(21) numerically far from the contact regions and match with this quasi-equilibrium profile as the boundary condition.

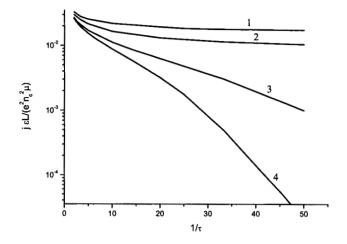


Figure 3: Temperature dependence of the 1D FET conductance in the linear regime  $(V_d = 0.1)$  for the same device as in Fig.2 at  $V_g = -12$  (1); -12.5 (2); -13 (3); -13.2 (4).

Since in our case  $\phi_c(x) < 0$  (or, in other words, the electron concentration is lower in the channel due to the absence of doping), we must obtain a lower absolute value of the cut-off voltage and a lower transconductance as compared to the previous subsection. For the same parameters as in Sec.5.1, the cut-off voltage  $V_g = -7.64$  as obtained by expanding Eq.(7) near the middle point instead of expression (19) useful only for  $n_c = N$ . Fig.4 presents the numerical results for the case of injecting contacts. Qualitatively IVCs have the same character as in Fig.2 but a weaker dependence on  $V_g$  and the temperature is seen. The above-threshold curve in Fig.5 ( $V_g = -6$ ) is, as in Fig.3, practically temperature-independent (the difference in the currents at  $\tau = 0.05$  and  $\tau = 0.2$  is less than 5%).

## 6. The role of contact geometry

## 6.1. 2D planar contacts

Due to a very weak screening in thin nanowires and nanotubes, the potential profile  $\phi^0(x)$  and hence all FET characteristics depend noticeably on the geometry of source and drain contacts  $^{8,10,30,38}$ . So far we have considered bulk, three-dimensional contacts (Fig.1A). In many cases contacts to a wire have not bulk but planar character representing highly conducting regions with macroscopic lateral sizes but very small thickness (Fig.1B). In this case the profile of electric field between source and drain

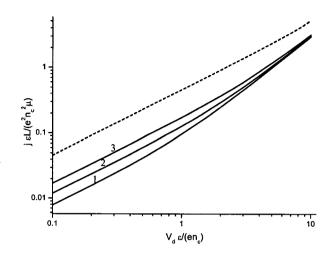


Figure 4: IVC of a 1D FET with d/L = 0.3 and injecting contacts at different gate voltages:  $V_g = -12$  (dashed line) and  $V_g = -13.2$  (solid lines) for the temperatures:  $\tau = 0.05$  (1); 0.1 (2), and 0.2 (3). (Curves for all three temperatures and  $V_g = -6$  coincide.)

differs drastically from that for bulk electrodes. To confirm this statement, it is enough to remember that in the absence of a gate the electric field between the bulk electrodes is uniform, whereas for the two-dimensional electrodes it has singularities near the contacts.

To find  $\phi^0(x)$  in 2D case, we must solve the Laplace equation in the system of coplanar source and drain semi-planes parallel to the gate plane. We split the total potential created by this system,  $\Phi(x, y)$ , into symmetric and antisymmetric part:  $\Phi(x, y) = \Phi_s(x, y) + \Phi_a(x, y)$  and find these parts separately from the Laplace equations with the following boundary conditions:

$$\Phi_s(x,0) = V_g, \quad \Phi_s(x > L/2, d) = 0, \quad \frac{\partial \Phi_s}{\partial x}(0,y) = 0; 
\Phi_a(x,0) = 0, \quad \Phi_a(x > L/2, d) = V_d/2, \quad \Phi_a(0,y) = 0$$
(22)

and then we find  $\phi^0(x) = \Phi(x, d)$ .

To solve these problems, we apply the conformal mapping

$$\frac{\pi z}{2d} = \ln\left(\sqrt{w} + \sqrt{w-1}\right) + \beta \sqrt{\frac{w-1}{w}}$$
(23)

transforming the first quadrant at the z = x + iy plane with the cut x > L/2, y = d into the upper semi-plane at the w = u + iv plane <sup>24</sup> so that the source electrode corresponds to the semi-axis u < 0, the semi-axis y > 0 — to the segment 0 < u < 1

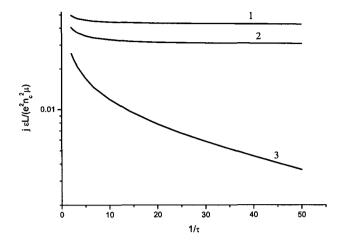


Figure 5: Temperature dependence of the 1D FET conductance in the linear regime  $(V_d = 0.1)$  for the same device as in Fig.4 at  $V_g = -6$  (1); -7.6 (2); -10 (3).

and the gate electrode — to the remaining part of u –axis. The parameter  $\beta$  in Eq.(23) is to be found from the equation

$$\frac{L}{d} = \frac{4}{\pi} \left[ \sqrt{\beta(\beta+1)} + \ln\left(\sqrt{\beta} + \sqrt{\beta+1}\right) \right].$$
(24)

It increases monotonically with L/d with the following asymptotes:  $\beta \simeq [\pi L/(8d)^2$  at  $L \ll d$  and  $\beta \simeq \pi L/(4d)$  at  $L \gg d$ .

In the (u, v) coordinate system the Laplace equations with the boundary conditions Eq.(22) can be easily solved:

$$\Phi_s(u,v) = V_g \left\{ 1 - \frac{2}{\pi} \operatorname{Im} \left[ \ln \left( \sqrt{u + iv} + \sqrt{u + iv - 1} \right) \right] \right\}; \quad (25)$$

$$\Phi_a(u,v) = \frac{V_d}{2\pi} \arctan\left(\frac{v}{u}\right).$$
(26)

Note that in Eq.(26) the argument of  $(\arctan x)$  is in the  $(0, \pi)$  interval. These equations along with Eq.(23) determine implicitly the potential profile created by two-dimensional electrodes.

Though we cannot transform analytically the solution Eqs.(25),(26) into the (x, y) coordinate system and obtain  $\phi_{s,a}^0(x)$  explicitly, some analytical results could be, nevertheless, obtained. The FET characteristics near the cut-off are determined by the concentration profile n(x) in the vicinity of the minimum of  $\phi(x)$ . We will perform expansion of  $\phi(x)$  in Taylor series near this point. For small  $V_d$  this is the point x = 0 which means that we need to know only  $\phi_s^0(0) \equiv \Phi_s(x = 0, y = d)$  and

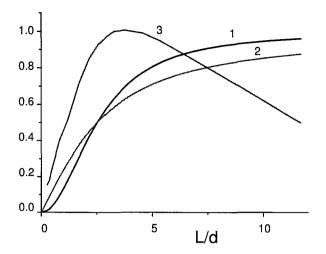


Figure 6: Dependence of (1) the transformation parameter  $u_0$  (see the text), (2) the channel potential  $\phi_s^0(0)$  at the minimum and (3) the curvature of the potential  $d^2\phi_s^0/dx^2(0)$  on the 1D FET geometry.  $\phi_s^0(0)$  is measured in the units of  $V_g$ ,  $d^2\phi_s^0/dx^2(0)$  — in the units of  $2V_g/L^2$ .

the second derivative of  $\phi_s^0$  in this point. In (u, v) coordinates the above-mentioned point is  $(u_0, 0)$  where  $0 < u_0 < 1$  and is determined by the equation

$$\arctan\sqrt{\frac{1-u_0}{u_0}} + \beta\sqrt{\frac{1-u_0}{u_0}} = \frac{\pi}{2}.$$
(27)

Fig.6 shows the dependence of  $u_0$  on the parameter L/a obtained from Eqs.(24),(27) and having the following asymptotes:  $u_0 \simeq [\pi L/(8d)]^2$  at  $L \ll d$  and  $u_0 \simeq 1-4d^2/L^2$ at  $L \gg d$ . By substituting this  $u_0$  and v = 0 into Eq.(25) we obtain  $\phi_s^0(0)$  also shown in a Fig.6. It has the asymptotes:  $\phi_s^0(0) \simeq V_g L/(4d)$  at  $L \ll d$  and  $\phi_s^0(0) \simeq$  $V_g[1-4d/(\pi L)]$  at  $L \gg d$ . The curvature  $d^2\phi_s^0/dx^2(x=0)$  was also calculated and presented at the same figure.

## 6.2. 1D wire-like contacts

It is appealing to fabricate the contacts to the 1D channel in the form of two thin wires perpendicular to the channel (see, e.g.,  $^{25}$ ). This is geometry of a 1D contact as it is shown in Fig.1C. If we assume these wires to be infinitely long (which means that their length considerably exceeds L) and have the radius  $a_c$ , then the potentials can be calculated relatively simply as the sum of potentials created by 4 cylinders (source, drain and their images in the backgate):

$$\phi_s(x) = V_g + \frac{V_g}{\ln(L/a_c)} \ln \frac{(x+L/2+a_c)(-x+L/2+a_c)}{\sqrt{4d^2 + (x+L/2)^2}\sqrt{4d^2 + (-x+L/2)^2}}; \quad (28)$$

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$$\phi_a(x) = \frac{V_d}{2\ln(L/a_c)} \ln \frac{(x+L/2+a_c)\sqrt{4d^2+(x+L/2)^2}}{(-x+L/2+a_c)\sqrt{4d^2+(-x+L/2)^2}}.$$
(29)

Calculations of the transconductance in the linear regime are based on the same formula Eq.(17) as in the Sec.4. The quantitative difference is in a particular profile of the  $\Psi(t)$  function. Though its expansion near the maximum is, of course, also quadratic and hence it gives qualitatively the same final result  $di/dg = A(g - g_0)^{-1/2}$ , the expansion coefficients are different. As a result, the cut-off voltage  $g_0$  and the coefficient A may differ considerably from the case of bulk contacts. The whole IVC, as before, must be found by numerical calculations taking into account the fact that for two-dimensional contacts not only  $\phi_c(x)$  but also  $\phi_g(x)$ have singularities near the contacts. Thus one has to match the numerical solution in the middle of the channel with an analytical quasi-equilibrium solution in the region near the contacts as described in Sec.5.2, even for the Ohmic contacts.

#### 7. Hysteresis and memory effects

The theoretical model considered in the previous sections gives a general physical picture and qualitative regularities describing electrical parameters of 1D FETs but, being general, cannot account for all specific features observed experimentally. For instance, some recent studies 26,27,28 demonstrated that IVCs of nanotube-based FETs have a strong hysteretic effect revealed as a difference in the threshold gate voltages measured for  $V_g$  swept in positive and negative direction. A similar hysteresis is known to exist for Si devices and exploited for the memory elements <sup>29</sup>. By analogy, it was supposed that these nanotube FETs may also become nonvolatile memory elements operating at the few-(single-)electron level even at elevated temperatures. In Si devices hysteresis is usually explained by generation/recombination of electrons at the traps in the oxide layer (the so-called slow surface states). In our case, we may expect a similar recharging stimulated by the channel-gate electric field (the Fowler-Nordheim effect). This field in quasi-1D-systems is  $\sim a^{-1}$ in the vicinity of channel and, hence, can be very high. One may therefore expect the memory effects to be observed at lower  $V_g$ , as compared to classical FETs. The described electron tunnelling to (or from) dielectric layer causes potential redistribution in the system resulting in a shift of the threshold voltage. Due to a low tunnelling probability, the characteristics time of corresponding charge transport may exceed the inverse frequency of  $V_g$  sweeping, which is consistent with the observed hysteresis.

For further phenomenological description we assume that the distribution of this charge is cylindrically symmetric. For FET model with a cylindrical gate (see, e.g., <sup>30</sup>) it is definitely the case. Moreover, we may expect this assumption to be also correct even in the planar gate geometry discussed in the previous sections if the nanotube/nanowire is completely buried in the oxide. According to the general expressions of Sec.2, we can claim that the shift of threshold voltage due to recharging of traps in the dielectric

$$\delta V_{g0} = \frac{e\delta N(0)}{C_t},\tag{30}$$

where  $\delta N(0)$  is the linear density of such charged traps taken at x = 0 since this point plays the role of a 'bottleneck' determining the offset of channel current.

The value of  $\delta N(0)$  is found from the generation-recombination equation describing recharging of traps through the Fowler-Nordheim mechanism. If the maximal possible  $\delta N(0)$  is limited by the total density of empty traps in a thin shell accessible for tunnelling electron,  $N_0$ ,<sup>‡</sup>then its dynamics is dictated by the equation

$$\frac{d\delta N(0)}{dt} = \frac{J\sigma}{e} \left[ N_0 - \delta N(0) \right].$$
(31)

Here  $\sigma \simeq 10^{-17} cm^2$  is the cross-section of the generation (and recombination) <sup>31</sup>, and we estimate  $N(0) = 10^{13}$  cm<sup>-2</sup> <sup>33</sup>. The Fowler-Nordheim current density depends on the electric field near the FET channel  $\mathcal{E}$ , which in turn depends on the potential and the radius of the 1D channel R (and logarithmically depends on the gate distance d):  $\mathcal{E} = \phi/(R \ln(d/2R))$ .

$$J = A\phi^2 \exp(-B/\phi) \tag{32}$$

where the constants  $A \simeq 10^5$  A cm<sup>-2</sup>V<sup>-2</sup> and  $B \simeq 150V$  are known for tunnelling in typical materials <sup>32</sup> and depend mostly on the effective mass of the carriers and the trap level.

Eq.(32) has been solved numerically and the result depends on the sweeping rate (SR) and the sweeping range of  $V_g$  that reflect the specifics of a particular experiment with a nanotube or nanowire FET. The physics of this dependence is clear: the slower  $V_g$  is swept and the larger is the sweeping range, the larger the density of injected electrons (cumulative charge in the substrate in our case), and thus the larger the hysteresis in accord with Eq.(30). The results of our modelling are presented in Fig.7. The potential of the ionized impurities creates an additional term (30) in the external potential as given by Eq.(7). This term is plotted in the figure as a function of the gate voltage. This extra term shifts the threshold voltage as given by expression (20). The shift is different for different direction of the gate voltage sweep, because the traps are charged/discharged when the voltage is swept up/down.

The dependence of the hysteresis width, H, on the sweeping rate is close to logarithmic. We explain this by the exponential dependence of the steady state solution of the Eqs. (31,32) on the electrostatic potential, then, the potential itself is roughly proportional to the  $\log \delta N$  which is proportional in turn to the sweeping rate. Similarly, the hysteresis increases with the sweeping range as shown in Fig.8.

<sup>&</sup>lt;sup>‡</sup>For large  $N_0$ , the maximal  $\delta N(0)$  can be limited not by the absence of empty traps but by the drop of the local channel-gate electric field making the tunnelling rate too small to be observed in real time.

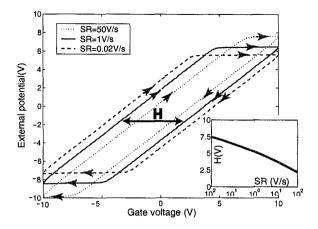


Figure 7: The potential induced by ionized traps vs. the sweeping rate of  $V_g$ . Inset: log-linear plot of the hysteresis width, H, vs the sweeping rate.

Following the theory of Sec.4, we can write the FET drive current density in a linear regime via the integral of the inverse quasi-equilibrium charge density, Eq.(16). Since in this section we are mostly interested in describing the effect of the hysteresis, for clarity of the presentation, we apply a toy model with the full axial symmetry of the cylindrical gate and trap potential. This approximation may though give a realistic estimate for the device with planar gate geometry which was discussed in the rest of the paper. This is because the transport at the threshold mostly depends on the potential profile at the middle of the channel, where it is almost flat. We note that in this model the effects of the fringe fields at the channel ends and all contact phenomena are fully neglected.

If all potentials have full cylindrical symmetry, the integration along the channel length is trivial and gives for the driving current density:

$$j = V_d \frac{e\mu}{L} (n_c + \Delta n_0(x)).$$
(33)

where  $\mu = 9000 \text{ cm}^2/\text{Vs}$ , d = 500 nm and  $L = 10d = 5\mu\text{m}$  is the effective length of the FET channel (the length over which the potential can be considered flat within the cylindrical model). We conclude that in the cylindrical gate model, the current in the linear regime is a linear function of the channel charge density as in a standard MOSFET. Substituting the parameters as specified above, we obtain the IVCs, shown in Fig.9.

## 8. Conclusions

The present work is devoted to the theory of nanowire and nanotube based transistor structures, which represents an important step towards developing a general theory of nanoscale 1D devices. In the framework of our problem we model a carrier

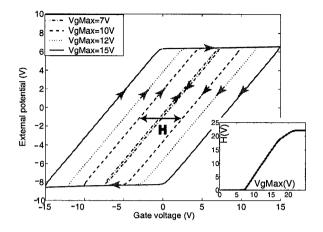


Figure 8: The potential induced by ionized traps vs. the sweeping range (at the sweeping rate 0.1 V/s). Inset: Hysteresis width vs. the sweeping range.

distribution and a conductivity in a quasi-1D channel placed between two metal electrodes over a backgate electrode. This structure is in fact a 1D FET. For details on the fabrication and experimental investigation of nanowire FETs in the recent years we refer to publications  $^{18,20,34}$ . To give an adequate theoretical description of basic characteristics of a 1D FET is the main task of our calculation. These results, with some restrictions, can be applied to such important object as a carbon nanotube FET  $^{22,35,36}$ . The mentioned restrictions are due to the fact that we treat the carrier motion in a channel within a drift-diffusion model while short carbon nanotubes are believed to have a ballistic conductivity  $^{8,13,37}$ . That is why the universal nanowire and nanotube model presented above is presumably applicable to the nanotube devices with a long enough channel only. We note that our theory in the part related to the induced potential profile is still applicable to any 1D device which is at the equilibrium (or very close to it) because the calculation of the equilibrium charge distribution does not depend on any assumption about the charge transport mechanism.

We focus in this paper on a universal analytical solution for the transport equations in a 1D channel under the drift-diffusion approximation, which has not been formulated previously. An essential difference for the 1D-FET model as compared with a standard planar FET model is due to the poor screening at the low dimensions. Thus, the channel resistance, which is shown to depend on the self-consistent charge density in the channel, can be more effectively controlled by the gate voltage. Although the operation principle of the 1D-FET is similar to the planar device, different electrostatics for the 1D channel results in a different behavior and in different device characteristics. For example, the transconductance at the threshold, unlike in a bulk FET, has a typical dependence  $\sim 1/\sqrt{V_g - V_{g0}}$ . With a lower (leakage) OFF currents observed recently in 1D-FET, this makes these devices very attractive

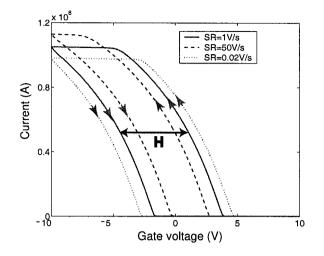


Figure 9: Current (in neglecting the contact resistance) vs. the gate voltage for different sweeping rates: 0.02, 1 and 50 V/s.

for electronic applications.

We have shown above that our transport model may have a straightforward generalization to a case of existence of movable/ionizable charges placed around the channel. This problem has a direct relevance for nanotube FETs and for a few of nanowire devices (to be discussed elsewhere). The model of the hysteresis, responsible for the memory effects in nanotube FETs, is presented. We calculated the typical IVCs taking into account the generation/recombination at the charge traps within a simple toy model (of a cylindrical gate) for an effective channel resistance. We note that a similar approach describes adequately the 1D FET with a chemically or bio-functionalized channel (to be published elsewhere).

#### Acknowledgments

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### CARBON NANOTUBE BASED NONVOLATILE MEMORY DEVICES

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The technology progress and increasing high density demand have driven the nonvolatile memory devices into nanometer scale region. There is an urgent need of new materials to address the high programming voltage and current leakage problems in the current flash memory devices. As one of the most important nanomaterials with excellent mechanical and electronic properties, carbon nanotube has been explored for various nonvolatile memory applications. While earlier proposals of "bucky shuttle" memories and nanoelectromechanical memories remain as concepts due to fabrication difficulty, recent studies have experimentally demonstrated various prototypes of nonvolatile memory cells based on nanotube field-effect-transistor and discrete charge storage bits, which include nano-floating gate memory cells using metal nanocrystals, oxide-nitride-oxide memory stack, and more simpler trap-in-oxide memory devices. Despite of the very limited research results, distinct advantages of high charging efficiency at low operation voltage has been demonstrated. Single-electron charging effect has been observed in the nanotube memory device with quantum dot floating gates. The good memory performance even with primitive memory cells is attributed to the excellent electrostatic coupling of the unique one-dimensional nanotube channel with the floating gate and the control gate, which gives extraordinary charge sensibility and high current injection efficiency. Further improvement is expected on the retention time at room temperature and programming speed if the most advanced fabrication technology were used to make the nanotube based memory cells.

*Keywords:* carbon nanotube; non-volatile memory device; FET; nanocrystal; quantum dot; floating gate; single-electron charging.

#### 1. Introduction

The rapid market expansion of personal computers and other consumer electronics such as digital cameras, mobile phones, MP3 players and personal data assistant devices, has triggered a continuing demand for nonvolatile electronic memories that are cheaper, faster, of higher storage density, and lower power consumption. For the past three decades, this has been achieved mainly by scaling of the physical dimensions of the devices following the technology roadmaps of the semiconductor industry [1]. The current technology node for flash memory, a mainstream nonvolatile memory in current market, has reached 90 nm, and is expected to scale down to 32 nm in the next couple of years. It is, however, becoming more and more difficult to continue this trend as we entered the nanoscale region due to the short channel effects in the scaling of metal-oxide-semiconductor field-effect-transistor (MOSFET) and the conflicting requirement for charging speed and retention time in the scaling of tunneling oxide. Researchers have been exploring new materials and cell structures to

overcome these difficulties and to extend the roadmap of flash memory. Discrete nanocrystal floating gate [2], crested tunneling barrier [3], oxide-nitride-oxide (ONO) stack [4,5] have been proposed to improve the tunneling efficiency and the charge retention. Ultrathin body silicon-on-insulator (SOI) [6] and FinFET [7] has been used to reduce the short channel effect and improve electrostatic coupling. Beyond the flash memory extension, researchers also started to investigate many emerging research memory devices that are not based on electronic charge storage, such as phase change, resistance change, ferroelectric, magnetic, and molecular memory [1].

Among various materials explored for non-volatile memory applications, carbon nanotube (CNT) has attracted great interest due to its unique geometry and excellent mechanical and electrical properties [8,9]. The unique features of CNTs have enabled researchers to conceive some novel memory concepts, such as shuttle memory and nanoelectromechanical memory, which do not apply to any other materials. On the other hand, those features also enabled us to explore the possibility to extend the current flash memory to its extreme limit by replacing silicon with semiconducting CNTs. This paper will give a review of different CNT memory devices that have been studied in recent years. The operation principles and experimental realization, as well as their technical merits and limitations, will be discussed. Focus will be on the carbon nanotube field-effect-transistor (CNTFET) based memory because it is the most intensively studied CNT memory device.

# 2. CNT shuttle memory and nanoelectromechanical memory

The first non-volatile CNT memory concept proposed is the "bucky shuttle" - a naturally ionized endohedral fullerene (also called "bucky ball") shuttling within a bigger fullerene or nanotube [10]. This idea is based on the unique geometry of a nanotube whose hollow inner space and closed ends define a perfect place to hold smaller molecules like a peapod [10,11]. The encapsulated endohedral fullerene can reside in one of the two stable energy states at the opposite ends of the hosting nanotube and be switched between these two positions by applying an electric field as shown in Fig. 1. There is, however, no promising scheme to read the states of such memories. To resolve this problem, a new version of "nanotube shuttle" memory device has been proposed [12,13]. This device is composed of two one-side capped outer single-walled nanotubes (SWNT) with aligned open ends and an encapsulated short nanotube shuttling between them (Fig. 2). Depending on which SWNT the encapsulated nanotube resides in, the electronic property of that side will change (partially becomes double-walled) [14,15] and this will enable the detection of the memory states. The encapsulated nanotube can be formed by annealing endohedral fullerenes [16,17]. The two outer SWNTs can be made by cutting a SWNT using lithography and etching technology [13]. The gap between the two open ends should be controlled small enough so that the encapsulated nanotube could not escape the system. Despite of the interesting theoretical simulation results, no experimental study has been done on the shuttle type CNT memories due to the difficulties to fabricate the cell itself and the electrical contacts.

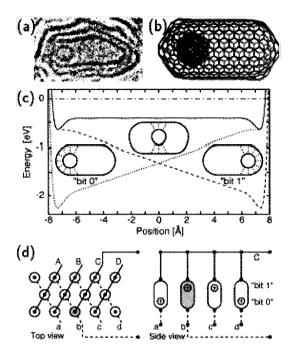


Fig. 1. Concept of "bucky shuttle" memory element. (a) and (b) Transmission electron micrograph and a model showing a fullerene in a short nanotube. (c) Position dependent energy of an endohedral fullerene  $K@C_{60}^*$  within an elongated fullerene  $C_{480}$  calculated by molecular dynamics simulation. The dash lines are under switching electric field. (d) "Buck shuttle" memory array concept. From reference [10].

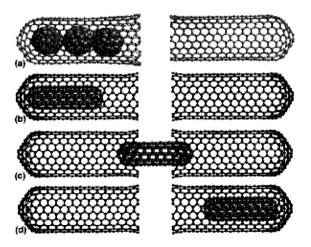


Fig. 2. A proposed carbon nanotube shuttle memory device. From reference [12].

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The second category of nonvolatile CNT memory is based on a miniature of electromechanical relay where the switching is realized by the elastic deformation of flexible CNT strings under an electrostatic force. An earlier proposed memory structure was nanotube cross bar array as shown in Fig. 3 [18]. A suspended CNT can be pulled towards another CNT below by applying electrostatic potentials with opposite signs between them. Once they are in touch, the strong van de Walls force can hold them together even with the removal of the voltage. The physical contact between two conducting CNTs gives an electrical ON state. If the two CNTs are both charged with a proper potential of the same sign (relative to the grounded substrate), the top CNT can be repelled away from the bottom CNT and thus break the electrical connection. This represents an OFF state. Although this idea works for single memory element (as already demonstrated experimentally in reference [18]), a simple cross bar array as shown in Fig. 3A will fail to function as a memory array if the number of the cross points increase because there is no cell selection mechanism in this architecture [19]. A recent revised version of the electromechanical CNT memory cell uses a fabric of CNTs as the top electrode and an embedded metal row as the bottom electrode [20,21]. The new structure can be fabricated using current lithography tools and is easy to integrate diode or transistor type selection devices. The drawback is the density of the memory cells will be much larger than the initial CNT cross bar array.

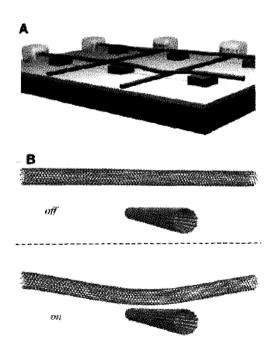


Fig. 3. (A) A proposed electromechanical CNT cross bar memory array. Lack of cell selection mechanism in this structure makes it unpractical for large array. (B) The ON and OFF states of the CNT cross bar memory element. From reference [18].

### 3. CNTFET based nonvolatile memory

Recent experimental and theoretical studies have shown that CNTFET device can outperform silicon MOSFET in many ways [22-25]. It has been listed in the International Technology Roadmap of Semiconductors as an emerging candidate succeeding silicon CMOS (complimentary metal-oxide-semiconductor) device [1]. In the non-volatile memory application, however, it is not a straight forward solution to simply replacing silicon MOSFET with CNTFET in a Flash cell without a significant change of the cell structure. Unlike the FinFET [7], whose channel is still considered bulky comparing with a CNT channel, the bulk floating gate in the present flash cell structure seems unlikely to be able to pull out the full advantage of the CNTFET considering the electrostatic coupling and the charge injection efficiency. On the other hand, recent studies on the nanotube chemical or biological sensors have hinted that the threshold voltage of a CNTFET is extremely sensitive to discrete electronic charges surrounding the CNT channel [26-30]. While the charges in these sensors are generated as a result of chemical or biological reactions, discrete charges can also be generated by other means such as using light [27] or charged polymers [28]. For the nonvolatile electronic memory, the charges need to be generated electrically and stay immobile around the CNTFET until it is removed by a reverse electrical pulse. It has been experimentally demonstrated that charges could easily be injected from CNTFET into traps or other discrete charge storage sites by applying a voltage on the control gate. The presence of nearby charges will shift the threshold voltage of the CNTFET and produce hysteretic behaviors of the drain current ( $I_d$  or  $I_{sd}$ ) as a function of the gate voltage ( $V_g$ ).

Hysteresis phenomena often observed in simple CNTFETs were mainly attributed to the injection and storage of charges into traps in the silicon oxide  $(SiO_2)$ , a common substrate for CNTFET device [31-33], although water and other molecules absorbed on the CNT surface or the CNT-SiO<sub>2</sub> interface can also contribute to the phenomena [34,35]. Fig. 4 shows such a simple CNTFET device made by a chemical vapor deposition (CVD) process and its memory effect [31]. The Isd - Vg curve shows a large hysteresis for this p-type transistor, with threshold voltage shift  $\Delta V_{th} \sim 6$  V when  $V_g$  is swept between + 10 V and - 10 V at room temperature. The threshold voltage shift is much smaller when measured at low temperature,  $\Delta V_{th} \sim 0.15 \text{ V}$ when charging voltage changes from -1 V to -5 V at 20 K [31]. This suggests that the charge injection is mainly through Poole-Frenkel conduction in the SiO<sub>2</sub> that is suppressed at low temperature. The charge retention of this device is poor, 5000 s at room temperature and 100 s at 20 K, despite of the very thick tunneling oxide (500 nm). A later report of a similar device made from dispersing arc-discharged SWNTs on a 100 nm SiO<sub>2</sub> has shown a retention time as long as 12 days [33]. In addition to the p-type transistors used the pre-mentioned studies, n-type ambipolar CNTFETs have also been shown memory effect with a retention time of 16 h [32].

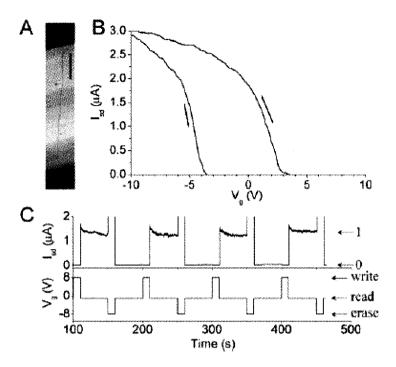


Fig. 4. (A) Atomic force microscopy (AFM) image of a SWNT connected with source and drain electrodes (dark contrast). The SWNT was grown on a heavily doped silicon substrate with 500 nm SiO<sub>2</sub>. The substrate works as back-gate for the CNTFET. Scale bar: 1 micron. (B)  $I_{sd} - V_g$  curves measured with source-drain bias ( $V_{sd}$ ) of 500 mV at room temperature. (C) Demonstration of memory functions of the CNTFET at room temperature. From reference [31].

Although a simple CNTFET can works as a memory device through storing charges in SiO<sub>2</sub>, the detailed charge injection process is still unknown. This causes uncertainty on the reliability and the retention capability of the device because the SiO<sub>2</sub> itself works as both tunneling barrier and storage media in such device and the trap density determines both the charge density and the leak current. To avoid this problem, Choi et al. used a SiO<sub>2</sub> – Si<sub>3</sub>N<sub>4</sub> – SiO<sub>2</sub> (ONO) stack to store charges in a CNTFET based nonvolatile memory device [36]. ONO is known low defect density, high break down voltage and good charge retention [5]. The high trap density in the nitride layer provides charge storage sites while the oxide layer provides high quality tunneling barriers. In the demonstrated device [36], a ONO stack with thickness of 7 nm, 7 nm, and 14 nm, respectively, was deposited on top of a laser ablated SWNT that was dispersed on a thermal oxide substrate and connected with source and drain electrodes. A top-gate was deposited on top of the ONO layer (Fig. 5a). The I<sub>sd</sub> – V<sub>g</sub> curves measured at 5 K shows threshold voltage shift of 2 V when V<sub>g</sub> sweeps between – 12 V and + 12 V. The retention time of the ONO-CNTFET device is shown to be better than 100 s at 5 K.

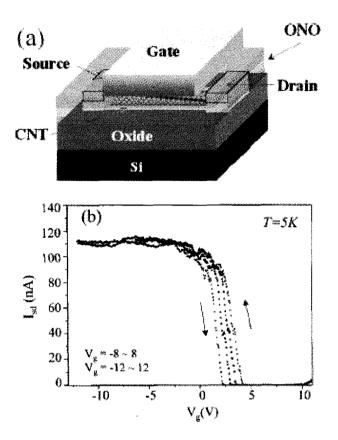


Fig. 5. (a) A top-gate ONO-CNTFET nonvolatile memory device; (b)  $I_{sd} - V_g$  curves measured ( $V_{sd} = 500$  mV) at 5 K. From reference [36].

Instead of using traps in dielectrics to store electronic charge, Ganguly et al. has recently demonstrated a CNTFET nonvolatile memory cell using metal nanocrystals as nano-floating gates [37]. A back-gated CNTFET with a thermal oxide layer of 100 nm were first made by using a CVD process. A 5 nm tunneling SiO<sub>2</sub> layer and a 1.2 nm Au thin film were then deposited on top of the CNTFET by electron-beam evaporation. The Au thin film self-assembled into a layer of nanocrystals during the electron-beam deposition [38]. A 30 nm passivation SiO<sub>2</sub> layer was then deposited using plasma-enhanced CVD. The final cell structure is shown in Fig. 6. Room temperature  $I_d - V_g$  measurements shows different  $V_{th}$ shifts when the device was pre-charged with different voltages (V<sub>CH</sub>) for 5 s before sweeping  $V_g$  from  $V_{CH}$  to + 2 V (Fig. 7). The higher  $V_{CH}$ , the larger  $V_{th}$  shift is. It should be noted that even in control device, where there is no nanocrystal, we still observed large Vth shifts. This can be explained by charge injection into the  $SiO_2$  layer as described earlier in the simple CNTFET device. Using a charging (or Vth shift) efficiency defined by a ratio of the difference of V<sub>th</sub> shifts and the difference of V<sub>CH</sub>, we can see that more charges were stored in the nanocrystal-CNTFET device ( $\Delta V_{th}$ /  $\Delta V_{CH}$  = 0.67) than in the control device ( $\Delta V_{th}$ /  $\Delta V_{CH}$  = 0.4). In order to verify that the extra charges were stored in the metal nanocrystals instead of

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oxide traps, low temperature measurements were performed. In the control device, very small  $V_{th}$  shift was observed with  $\Delta V_{th} / \Delta V_{CH} = 0.08$  at 10 K (Fig. 7c), indicating that the oxide traps were inactive at this temperature. This result is also consistent with the ONO device where  $\Delta V_{th} / \Delta V_{CH}$  is about 0.02 at 5 K [36]. For nanocrystal-CNTFET device, a large  $\Delta V_{th} / \Delta V_{CH}$  of 0.5 was observed at 10 K, which was attributed to the charge injection into nanocrystals. The nanocrystal-CNTFET memory device demonstrated a retention time better than 6200 s at 10 K, but only about 800 s at room temperature. The higher charge leakage at room temperature is attributed to the poor quality of evaporated tunneling oxide in which trap-assisted leakage current is thermally activated according to the Poole-Frenkel model.

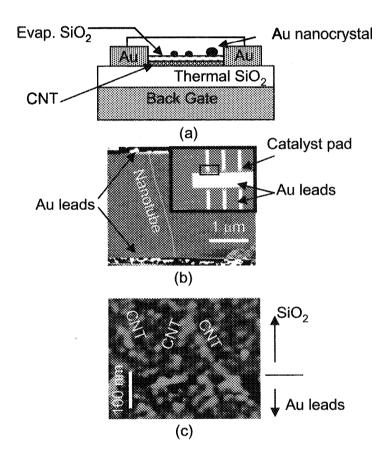


Fig. 6. (a) A cross-section illustration of the nanocrystal-CNTFET nonvolatile memory device; (b) AFM image of the top surface of a CNTFET device; the inset is an optical micrograph showing the layout of the test devices where the bright contrast indicates Au source and drain electrodes. The images were taken before deposition of metal nanocrystals. (c) AFM image showing formation of Au nanocrystals on SWNTs and substrates (before deposition of capping oxide layer). From reference [37].

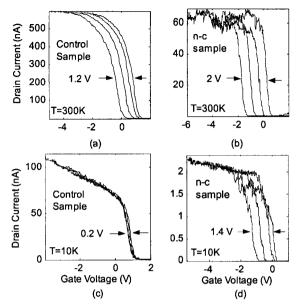


Fig. 7.  $I_d - V_g$  curves measured by sweeping  $V_g$  from charging voltage  $V_{CH}$  to 2 V for (a) CNTFET without nanocrystals at 300 K,  $V_{CH} = -5$  V, -4 V, -3 V, -2 V; (b) nanocrystal-CNTFET at 300 K,  $V_{CH} = -6$  V, -5 V, -4 V, -3 V; (c) CNTFET without nanocrystals at 10 K,  $V_{CH} = -4.5$  V, -4 V, -3 V, -2 V; (d) nanocrystal-CNTFET at 10 K,  $V_{CH} = -5.4$  V, -4 V, -3 V, -2 V. From reference [37].

#### 4. Electrostatics and charging efficiency

The CNTFET based nonvolatile memory devices, however primitive they are, have large threshold voltage shift with relatively low programming voltage. This is attributed to the ultimate charge sensibility (which will be further discussed in the next section) and the high charging efficiency. The advantage of high charging efficiency originated from the unique geometry and size of the CNT channel. Comparing with the tradition flash memory device where the control gate and the two-dimensional (2D) Si channel form a parallel capacitor with uniform electric field between them, the CNTFET based device has a highly non-uniform electric field distribution with strong field enhancement at the CNT/SiO<sub>2</sub> interface. This high local electric field was used to explain the effective charge injection from CNT into SiO<sub>2</sub> or nitride layer through Fowler-Nordheim mechanism [31,36,39]. The unique geometry of the CNT also allows the effective charging of a nano-floating gate in a back-control gate configuration [37]. Fig. 8 shows a simulated electric field profile in a model device where a 2 nm diameter SWNT (with a constant potential 5 V) and a 6 nm diameter metal nanocrystal (not charged) are placed above a grounded control gate [40]. The control oxide between the CNT and the control gate is 20 nm and the tunneling oxide between the nanocrystal and the CNT is 4 nm. The simulation shows that the field maximum is at the CNT/SiO<sub>2</sub> interface where the intensity is comparable with the break down field (~ 1000 MV/m) of SiO<sub>2</sub>. The strong fringe field that wraps around the CNT makes the difference much less important for a nanocrystal to be placed above or below the CNT. When the CNT is set to a positive voltage relative to the control gate, all local electric field lines point out from the CNT. In another word, as long as the nanocrystal is close to the CNT, the local field between them is always pointed from the CNT to the nanocrystal regardless of their positions relative to the control gate. This field could inject holes into (or withdraw electrons from) the nanocrystal from (to) the CNT. This is the reason why the back-gated nanocrystal-CNTFET device has shown excellent charging efficiency even with a relative thick control oxide layer (100 nm in the experiment) [37].

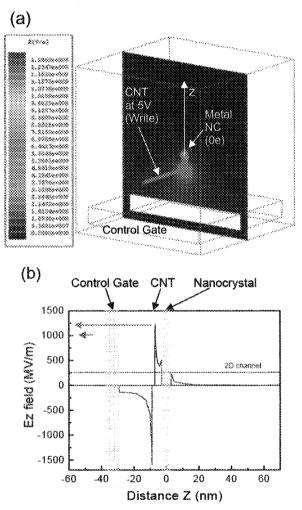


Fig. 8. (a) Cross sectional electric field profile in a model nanocrystal-CNTFET device. The color scheme represent the intensity of the electric field listed on the left side of the graph. The control gate is grounded. (b) Line profile of electric fields along the z-axis as indicated in (a). Strong field enhancement near the CNT/SiO<sub>2</sub> interface is presented. The maximum field pointing to the nanocrystal is indicated by the top arrow. The short bottom arrow indicates the breakdown field of SiO<sub>2</sub>. From reference [40].

## 5. "Bottleneck" effect and single-electron CNT memory

Single-electron memory has been an ultimate goal for electron charge based memories. Realization of the single-electron memory requires both the capability to store charge at a single-electron level and the capability to detect the single-electron. Single-electron charging can only occur in a system where the coulomb energy is larger than the thermal energy:  $E_c = e^2/2C \gg k_B T$ , where e is the electron charge, C the capacitance,  $k_B$  the Boltzmann constant, T the temperature [41]. A nanocrystal, or a quantum dot as named more generally, is good for single-electron storage because its small size makes the capacitance small and therefore increases the electrostatic charging energy so that single-electron charging could occur at a realistic temperature. An electron can only be added (or removed) to a quantum dot with a minimum energy change of  $\Delta E = (Q+e)^2/2C - Q^2/2C$ , where Q is the charge already in the quantum dot. This effect is called Coulomb blockade [41]. Since electrons can only be added or removed with an integer number, the system energy always changes in a discrete way.

Detection of single-electron level charge in a nano-floating dot could be done using a single-electron transistor (SET) [42], although fabrication of a SET that works at higher than liquid helium temperature is a big challenge. Another easier way to detect single charge is using a FET with a narrow channel width [6,43-45]. The requirement of a narrow channel is to avoid current percolation. As illustrated in Fig. 9, current in a 2D channel will follow a path of the least barrier height in a non-uniform potential field. It is therefore difficult to use a 2D channel to detect a single-dot charge. For a very narrow channel, however, there is only one path that the current could go and therefore the current can be significantly modulated by a single-charge close to the channel. This phenomenon is called "bottleneck" effect [6]. Obviously, the narrower the channel, the more significant the "bottleneck" effect is. This explains the ultra-high charge sensitivity of CNTFET where the CNT channel is an almost ideal 1D channel. This allowed the observation of single-electron charge or discharge events in many CNTFET based memory devices [31,36,37].

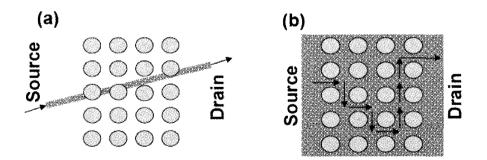


Fig. 9. Schematic illustrations of (a) 1D channel and (b) 2D channel (dark gray) in an array of potential wells of discrete charges (light gray) [40].

Both low-temperature and room temperature measurements of nanocrystal-CNTFET memory device have provided clear evidence of single-electron charging effect [37,46]. The  $I_d - V_e$ curves of different charging voltage show kinks at the transition region, which cause the curves to aggregate and form eye-opening patterns (Fig. 10a). A plot of the Vg values at a given  $I_d$  in the transition region shows a discrete  $V_g$  distribution with an interval of ~ 100 mV although  $V_{CH}$  changes with a fixed step (Fig. 10b). A careful analysis of each  $I_d - V_g$  transition curve indicates that a kink actually breaks the curve into two segments of the same slopes. This is equivalent to shifting the original  $I_d - V_g$  curve to another curve with  $V_{th}$  of ~ 100 mV higher than the original one (Fig. 11b). This  $V_{th}$  shift is attributed to the single-electron discharge event during sweeping of  $V_g$  from the  $V_{CH}$  to + 2 V in the experiments [37]. Due to Coulomb blockade effect, the Vth shift caused by the single-electron discharge only takes discrete values, which is also the physical origin of the eye-opening pattern and discrete transition voltage distribution for different V<sub>CH</sub>. A simulation of the nanocrystal-CNTFET device using non-equilibrium Green's function method has predicted a  $V_{th}$  shift of 50 ~ 90 mV for a single-electron charge, in good agreement with the experiment result (Fig. 11a) [46]. The step-like threshold voltage shifts due to the single-electron level charging effect provide an opportunity for multi-level operation of the CNT memory device.

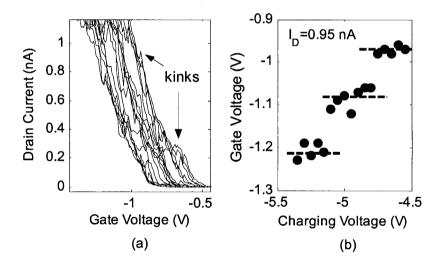


Fig. 10. (a)  $I_d - V_g$  curves measured at 10 K with  $V_{CH}$  advancing from - 5.40 V to - 4.55 V in 50 mV steps. (b) Plotting of  $V_g$  extracted from (a) at  $I_d = 0.95$  nA indicates a discrete transition voltage shift with an interval of ~ 100 mV due to the single-electron charging effect in nanocrystals. From reference [37].

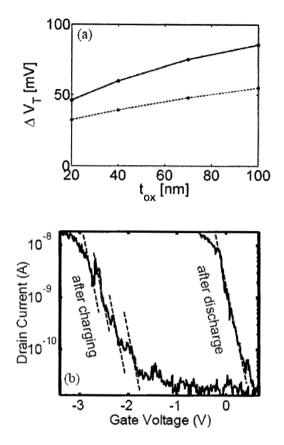


Fig. 11. (a) The simulated  $V_{th}$  shift due to a single-electron charging on point dot 5 nm (solid line) and 9 nm (dashed line) above a CNTFET (200 nm channel length, 0.5 eV CNT band gap, 0.12 eV Schottky barrier height with source and drain for electrons). The x-axis is the back-gate oxide thickness. (b) Room temperature measurement of a nanocrystal-CNTFET memory device right after charging (the curve on the left) and fully discharged (the curve on the right). The sub-threshold slope (dashed line) should be the same in both curves. The  $I_d - V_g$  curve for the charged device shows a series of threshold voltage shift of 100mV ~ 200mV due to discharge events during measurements. From reference [46].

#### 6. Conclusion

Experimental and theoretical investigation of CNT based nonvolatile memory cell structures, especially CNTFET based devices, has demonstrated distinct advantages over traditional 2D cells, such as lower programming voltage and single-electron level storage/detection. Those merits are attributed to the unique geometry, size, as well as the excellent physical properties of CNTs. On the other hand, there are still many questions remained to be answered. For example, could a CNTFET based memory devices reach a retention time comparable with that of the current flash memory (~ 10 years) [1]? It is understandable that the experiments so far have not used the most advanced process tools in the semiconductor industry, which could

result in very low quality of tunneling oxide and cause the deterioration of the retention time [37]. However, a theoretic analysis of such problem is apparently necessary to predict the performance limit of an ideal CNTFET memory device. In addition to the device structure itself, there are many other challenges in the material side that could prevent the application of CNT based memory devices. One major challenge is that CNTs are produced as a mixture of different types, metallic or semiconducting. Most device applications require a single type of nanotubes, for example, pure semiconducting tubes for CNTFETs. Another big challenge is that CNTs as molecular nanomaterials are very hard to be handled using traditional top-down fabrication technology in semiconducting industry. This obstacle also exists for other electronic applications of CNTs, such as CNTFETs in logic circuits. A novel bottom-up approach, such as type-selective self-assembly, is needed for practical high-volume manufacturing of CNT based electronic devices.

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# SINGLE-WALLED CARBON NANOTUBES: APPLICATIONS IN HIGH FREQUENCY ELECTRONICS

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In this paper, we review the potential applications of single-walled carbon nanotubes in three areas: passives (interconnects), actives (transistors), and antennas. In the area of actives, potential applications include transistors for RF and microwave amplifiers, mixers, detectors, and filters. We review the experimental state of the art, and present the theoretical predictions (where available) for ultimate device performance. In addition, we discuss fundamental parameters such as dc resistance as a function of length for individual, single-walled carbon nanotubes.

Keywords: Nanotube; interconnect; amplifier; antenna.

## 1. Introduction

The development of carbon nanotube synthesis, both for single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs), and of nanotube device physics has been rapid in the previous decade. The sphere of potential applications is broad due to their superior mechanical, thermal, and electrical properties. These have been reviewed in several recent monographs[1-7], as well as other manuscripts in this volume. However, an intriguing sphere of application which has until recently received relatively minor attention is in the area of high speed (RF, microwave, mm-wave, and THz) electronics. At first glance, the idea of combining nanotechnology with RF circuitry may seem to be a rather poor match, due to the typically high impedance of nano-electronics devices. However, the intrinsic speed limit of carbon nanotube devices can be very high, up to the THz range, so that on further reflection it seems potentially feasible to fabricate high speed devices and ultimately systems out of carbon nanotubes. The topic of this paper is to discuss how far along we are on the road to this goal, and in what manner it makes sense to even continue development of the technology, at least for high speed systems. Since the progress in synthesis has been very rapid, it is our point of view (at least for this review) that one should evaluate the ultimate potential of the technology, assuming the problems of economical fabrication could be solved.

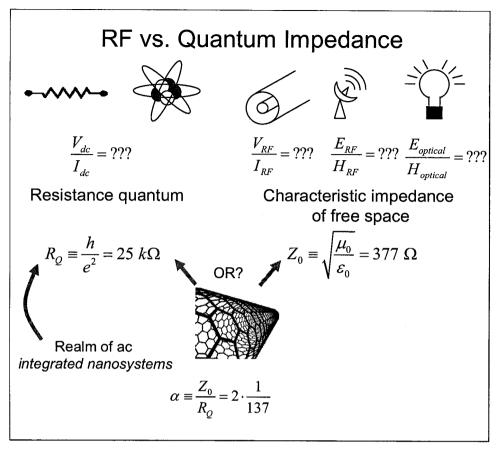


Fig. 1: Impedance matching and AC nanosystems.

### 2. AC Nanosystems

In RF waveguides, the ratio of the RF voltage to the RF current is of order the characteristic impedance of free space, i.e. 377  $\Omega$ . The ratio of the RF electric field to the RF magnetic field in free space plane waves is also of order 377  $\Omega$ . (The same is true for optical plane waves, as well.) On the other hand, nano-electronic devices such as resistors with dimensions of order the de Broglie wavelength of the electrons (typically the Fermi wavelength) have dc resistance values of order the resistance quantum[8, 9]  $h/e^2 = 25 k\Omega$ . The ratio of these two impedances is known as the fine structure constant  $\alpha$ , and is dependent on only three fundamental constants of the universe: the charge of the electron e, the speed of light c, and Planck's constant h. Therefore, there is an apparent built-in impedance mismatch between nanotechnology and RF. This mismatch has occupied the single-electron-transistor community for many years[10], and is now germane to the issue of nanotube based devices.

A general question thus arises: If one is interested in nano-electronic devices clocked at GHz or higher frequencies, to which domain do they belong: The quantum resistance domain, or

the free space impedance domain? It appears that there is no general answer to this question. However, we can make the following general claims: First, if an individual nano-device is to talk to the outside world, it will need to drive an impedance of order the characteristic impedance of free space. In this case, the impedance matching problem must be dealt with and cannot be ignored.

However, a paradigm we have recently advocated[11] is one of *integrated nanosystems*, in which nanotubes and nanowires are used both as the active elements and as the interconnects. In this case, the devices can all be dealt with in the realm of the resistance quantum, and still operate at ultra-high speeds. Such a paradigm is worth further investigating, but our conclusions will become clearer on this issue below.

# 3. SWNT electronic properties

The electronic properties of SWNTs vary, depending on their diameter and chirality[12]. The chirality determines whether the nanotube behaves as a metal or semiconductor. Experimentally, metallic nanotubes are typically distinguished by the absence of a dependence of the small bias conductance on a gate voltage. Similarly, semiconducting nanotubes have a conductance that depends strongly on the gate voltage. The band-gap of semiconducting nanotubes is related to the diameter through the  $E_g = 0.9 \text{ eV/d[nm]}$ , where d is the diameter in nm.

# 4. Synthesis

Since the original development of chemical vapor deposition (CVD) for nanotube synthesis from lithographically defined catalyst pads was developed in 1998[13], many groups around the world have continued to focus on using CVD for synthesis. In this section, we focus on a particular metric, that is the synthesis of relatively long single-walled carbon nanotubes. The reason, as will become clear below, is that nanotubes may have a role to play as interconnects and the synthesis of long tubes is a necessary step in that direction. Additionally, long SWNTs allow one to measure the resistivity without worry about contact resistance effects. In Fig. 2, we show an SEM image (from ref. [14], with permission) of an electrically contacted, 0.4 cm long SWNT synthesized in our labs.

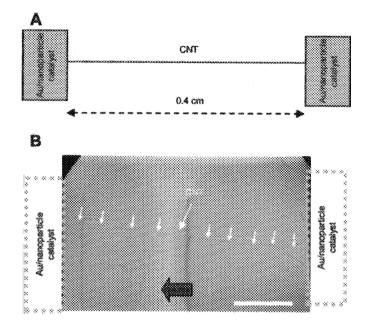


Fig. 2: Electrically contacted, 0.4 cm long SWNT, from [15].

In Fig. 3, we show a plot of length vs. year of electrically contacted, individual SWNTs (adapted from [15], with permission). (Data for figs. 3,4 from references [14, 16-37].) The progress has indeed been rapid. In addition, the tubes grown in CVD are highlighted in red, indicating that the growth technique has had a significant impact on the synthesis of long nanotubes. In Fig. 4, we show the length vs. year of all individual SWNTs. The electrically contacted SWNTs are circled in red. The progress has been about an order of magnitude increase in length per year. Such progress is rapid, even by the modern standards of electronics technology. It remains to be seen if and when such progress will plateau.

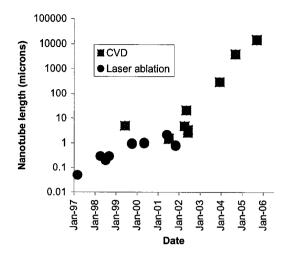


Fig. 3: Electrically contacted individual SWNT length vs. year.

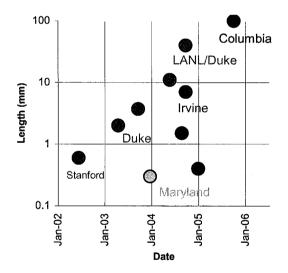


Fig. 4: Individual SWNT length vs. year.

# 5. Single walled nanotube DC resistivity

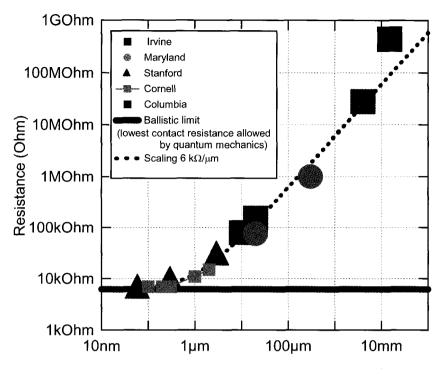
A nanotube can be considered a one-dimensional conductor, even at room temperature. It is by now well established[8, 9] that it is not possible to measure the resistivity of a 1d conductor using a four terminal measurement: any terminal attached to the conductor destroys the one dimensional nature of the conduction. Therefore, one can only perform a two-terminal measurement, and the contact resistance must be addressed.

For 1d systems that are in the ballistic limit (i.e. length less than the mean free path), the contact resistance is always greater than or equal to  $h/e^2 = 25 \text{ k}\Omega$ . In SWNTs, this number is modified by a factor of 2 for band structure degeneracy and a factor of 2 for spin[12], so that the lowest possible resistance a SWNT can have (when it is shorter than the m.f.p.) is  $h/4e^2 = 6 \text{ k}\Omega$ . However, in cases where the contact is poor (for example, if there is a Schottky barrier at the metal/nanotube interface), the resistance can be and typically is much higher. Recent work has shown that use of Pd as the contact material allows the theoretical limit to be reached, at least for very short SWNTs[38-40]. Prior to this, the more commonly used metal was Au and gave resistances of order M $\Omega$ , which was due to the poor contact.

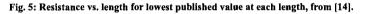
On the other hand, if the nanotube is long compared to the mean-free path, then the resistance will have a component that scales linearly with length. Exactly how long is the mean free path in a SWNT? This question has not been definitively answered, but by plotting the resistance vs. length for tubes of a variety of different lengths, one can get a reasonable estimate. To date, no studies have been published investigating this in full detail, so we are forced to use results from the literature, which will be expected to have a variation due to different processing conditions, different nanotube diameters, different measurement temperatures, and different species (i.e. metallic or semiconducting). Although the amount of data on nanotubes in the limit that the contact resistance is small is not large (there are only a few publications), the curve plotted in Fig. 5 (adopted from ref. [14], using data from refs. [14, 35, 38, 40-43]) shows a remarkably consistent trend: nanotubes with length less than about 1 micron can approach the ballistic limit. On the other hand, nanotubes with length greater than about 1 micron have a resistance per unit length of about 6 k $\Omega/\mu$ m. This indicates a mean-free path of about 1 µm, since (neglecting the contact resistance) the equation for the m.f.p. in 1d diffusive conductors is[8]:

(1) 
$$R_{dc} = \frac{h}{4e^2} \frac{L_{nanotube}}{l_{m,f,p}}$$

Remarkably, this indicates as 3d resistivity (assuming a diameter of 1.5 nm) of 1.1  $\mu\Omega$ -cm, which is lower than *bulk* copper (which has a value of 1.7  $\mu\Omega$ -cm). Thus, if a tightly packed array of SWNTs could be synthesized economically, the material would be a potentially disruptive technology for interconnects in integrated circuits. This motivates our discussion of the high frequency properties of single walled nanotubes as conductors.



#### Length (m)



#### 6. Metallic nanotubes as interconnects: RF properties (theory)

The RF circuit properties of a 1d conductor were originally discussed by Wesstrom[44], who developed a transmission line description. However, at the time the technology to experimentally address the concepts was lacking. In a related set of papers, theoretical physicists have been considering the ac impedance of 1d conductors from the Luttinger liquid point of view for over a decade [45-51]. We have recently applied the concepts of transmission line theory to develop a general RF circuit model for a single walled nanotube[52-55]. Salahuddin has generalized this approach to include multi-mode quantum wires [56]. Such a circuit model consists of distributed electrostatic capacitance and magnetic inductance, just as a classical transmission line. However, the model also includes quantum capacitance and kinetic inductance, which are absent in a classical transmission line. These extra elements describe a transmission line with characteristic impedance of order the resistance quantum, and a wave velocity of order c/100. Thus, the use of nanotubes as interconnects can allow one to stay in the realm of the resistance quantum even for transmission line work, and avoid the problems of impedance matching of active devices to the characteristic impedance of free space. Fig. 6 shows the equivalent RF circuit model for a SWNT over a highly conducting ground plane, neglecting damping (from Ref. [52], with permission).

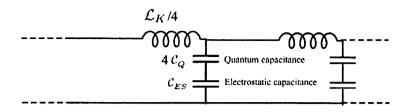


Fig. 6: RF circuit model for a SWNT, neglecting damping, from [52].

From the above section, we have a reasonable estimate of the dc resistance per unit length of about 6 k $\Omega/\mu m$ . Thus, if the ac damping is the same as the dc damping, the equivalent circuit model should include a resistance per unit length as well.

It may appear that the kinetic inductance is a problem for slowing down signal propagation on a nanotube. However, by comparing the kinetic inductance per unit length to the resistance per unit length, one comes to the conclusion that the resistive impedance will be more important than the inductive impedance for frequencies below about 200 GHz, at least for the 6 k $\Omega/\mu$ m number quoted above. These issues have also been recently discussed in Ref. [56]. For *integrated nanosystems*, this may result in some propagation delay.

A more critical issue to the propagation of information on nanotubes it that of dispersion, which will appear in any resistive system (including Cu) with capacitance. In fact, the resistivity of Cu is higher than that of nanotubes, so it is still possible that the dispersion on nanotubes is better than on Cu of the same dimensions, although this remains to be investigated more thoroughly. In Fig. 7, we plot our calculations of the real nanotube impedance vs. frequency for a realistic length of 100  $\mu$ m and resistance per length of 1k $\Omega/\mu$ m. It is clear that the impedance is undergoing significant frequency dependence (i.e. dispersion) at around the technologically relevant frequency of 1 GHz. This issue still needs to be addressed in more depth based on the application in mind, but our general circuit simulation techniques[52-55] should allow for modeling of the electrical properties at high frequencies.

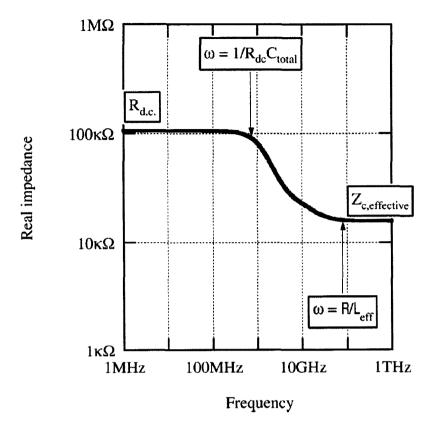


Fig. 7: Simulated real impedance for a 100  $\mu$ m long SWNT, assuming a resistance per unit length of 1 k $\Omega/\mu$ m.

#### 7. Metallic nanotubes as interconnects: RF properties (experiment)

Although the models provide some interesting intellectual exercises in understanding the interaction of microwave signals with 1d quantum systems, the fact remains that very few experiments to date have been performed to validate the proposed models. We recently measured the ac conductance of a 1  $\mu$ m and 25  $\mu$ m long SWNT (allowing both diffusive and ballistic transport to be probed), in both the low electric field and high electric field limit, up to 10 GHz. Prior work has demonstrated that the high electric field current in a metallic SWNT saturates at around 25  $\mu$ A[57]. There, it was shown that the saturation behavior is due to a modified mean-free-path for electrons when the electric field is sufficient to accelerate electrons to a large enough energy to emit an optical phonon. This effect was studied more quantitatively with similar conclusions in [39, 41].

In our recent RF measurements, we measured the change in the RF conductance as a function of bias voltage, and found no frequency dependence out to 10 GHz. The central results are plotted in Fig. 8 (from Ref. [58], with permission.) This work demonstrated clearly that nanotubes can carry current up to 10 GHz just as well as at DC, which is clearly significant.

To date no time-domain studies have been performed on nanotubes as interconnects, and no experimental studies on dispersion have been performed. Thus, while the promise is clear, there is still much work remaining to be done to validate the technology for RF applications in interconnects.

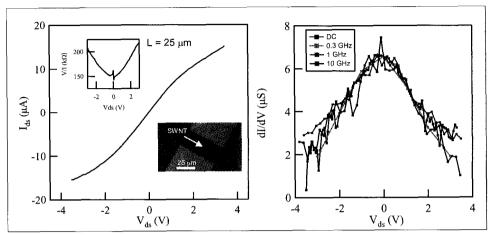


Fig. 8: I-V curve of 25 µm long SWNT and RF and DC conductance vs. V<sub>ds</sub>, from [58].

#### 8. Nanotube transistors: Cutoff frequency (theory)

A general figure of merit for any transistor technology[59] is the cutoff frequency  $f_T$ . In general, this can be limited by two timescales: an RC time, and a capacitance over transconductance time. For a SWNT field effect transistor (FET), the typical device geometry is shown in Fig. 9 below[60, 61], from Ref. [11] with permission. The on-state resistance of a SWNT FET is limited to  $6 k\Omega$  (h/4e<sup>2</sup>) or higher. This is quite a high resistance compared to 50  $\Omega$ , so that the impedance matching and parasitics are a significant issue. Nonetheless, the intrinsic performance of the device is expected to be quite fast.

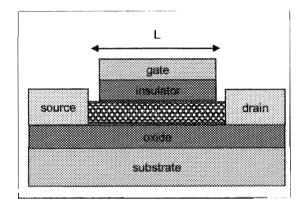


Figure 9: Typical geometry for a SWNT FET., from [61].

The intrinsic capacitance is typically of order 10s of aF. Therefore, the RC time for the intrinsic capacitance is extremely fast. The transconductance over the capacitance is the limiting factor. Here, measured transconductance values (which have been in the 10  $\mu$ S range) also give rise to an extremely high intrinsic speed limit. Based on these arguments, we predict semi-phenomenologically a cut-off frequency of 80 GHz/L<sub>gate</sub>[ $\mu$ m], where L<sub>gate</sub> is the gate length in  $\mu$ m. This prediction was independently derived by more rigorous simulations recently[62]. Thus, for sub-micron gate lengths, THz cutoff frequencies may be possible. In Fig. 10, we plot the predicted intrinsic cutoff frequency vs. gate length, reproduced from Ref. [11], with permission.

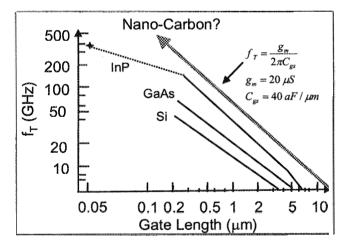


Figure 10: Cut-off frequency vs. gate length, from [61].

In order to quantitatively ascertain the effects of parasitics on realistic device performance, an effective circuit model for the device in the absence of parasitics is necessary. We recently proposed such a circuit model[11], and it is shown in Fig. 11. Here, by taking into account reasonable parasitics, we have predicted that the cutoff frequency for a typical example of a

 $0.1 \ \mu m$  gate length is about 10 GHz. Thus, the effects of parasitics are extremely important in SWNT FETs.

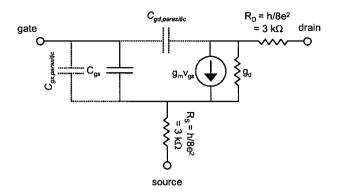


Figure 11: Small signal circuit model for SWNT FET, from [61].

#### 9. Nanotube transistors: High frequency performance (experiment)

To date, only relatively few experiments have been performed on the high frequency properties of SWNT FETs. In 2003, we demonstrated that the small-bias source-drain 2.6 GHz conductance of a back-gate SWNT FET depended on the dc gate voltage[43]. This was performed by constructing an off-chip LC impedance matching circuit out of discrete components. That work was performed at cryogenic temperatures, where Coulomb blockade effects were also significant. More recently, we have demonstrated that the room temperature 1 GHz source-drain conductance at both low and high dc source-drain bias voltages was the same as the dc conductance of a back-gated SWNT FET, after the parasitics were subtracted from the measurement[63]. These measurement results are shown in Fig. 12 below.

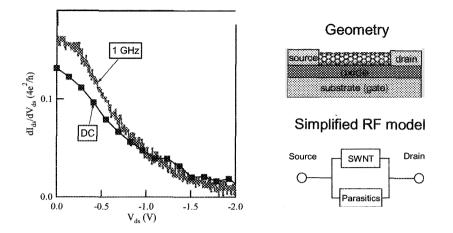


Fig 12: DC and AC source-drain dynamical conductance of SWNT FET, from [63].

In the time-domain, IBM has performed the first and so far only pulsed experiments[64], which show performance with sub- $\mu$ s speed, again limited by parasitics, as we discussed above.

Thus, the experimental state of the art of SWNT FETs for high frequency applications is still in its infancy. While the intrinsic device cutoff frequency can by in the THz range, significant challenges remain, in particular the issue of the parasitic capacitances, to achieve this potential performance. One potential solution is to use aligned array SWNT FETs, discussed next.

## 10. Array devices

One possibility for impedance matching is to fabricate aligned array devices. We show this basic concept in Fig. 13 below, from [65]. To date such a vision has been difficult to achieve, since in practice techniques to synthesis aligned arrays have too large of a pitch (typically larger than 10  $\mu$ m[36]), and also do not produce purely semiconducting nanotubes. If metallic nanotubes are present, the device will not turn completely off. Recent work on random mixtures of metallic and semiconducting nanotubes has been performed along these lines[66]. However, such an avenue holds promise for improving impedance matching for nanoscale electronics, in spite of the technological fabrication challenges.

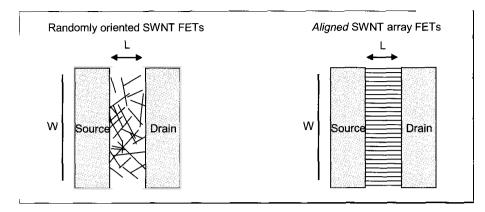


Fig 13: Concept for aligned array FETs, from [65].

## 11. Non-linear devices: Mixers and detectors

While transistor linear response data has been difficult to measure due to the impedance mismatch and effect of parasitics, device non-linear performance has been more clearly studied. A simple, straightforward experiment to study device non-linear performance is to apply an ac voltage to either the gate or the drain, and measure the induced dc current as a function of the ac frequency. In such a study, the nanotube performs as a non-linear detector (or a homodyne mixer) of RF voltages. Such studies probe whether the non-linearity in the transistor I-V curve persist up to high frequencies, and also give some quantitative information about parasitics.

IBM presented studies of these kinds initially on back-gated SWNT FETs up to 580 MHz[67, 68], and was limited by parasitics in going higher in frequency. Recently, Cornell has extended these studies to top-gated SWNT FETs, and measured results up to 50 GHz[69]. Interestingly, they observe a roll-off in the device response as a detector at around 10 GHz, which is exactly where we predicted parasitics would be important for linear device response. Thus, device non-linearities persist to microwave frequencies and possibly beyond, but impedance matching and parasitics are still critical to quantify, understand, and overcome.

## 12. Nanotube antennas

One final area of potential application is in the use of nanotubes as antennas[70, 71] antennas. So far in the RF and microwave, no experiments have been reported on this topic. However, there have been some theoretical developments. The essential idea is captured schematically in Fig. 14 below (from Ref. [72]). This idea could be useful for any application in which wireless contact to a nanoscale device is required, e.g. nano-scale sensors.

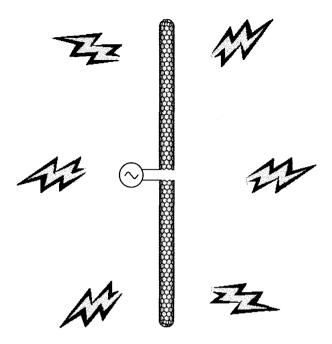


Fig 14: Concept for a nanotube dipole antenna, from [72].

One of the most fundamental parameters of any antenna is the current distribution on the antenna. This determines the radiation pattern, the radiation resistance and reactance, and many other properties of interest. Modern work on antenna theory is typically numerical because of the lack of analytical solutions. In contrast, early work on antenna theory (including some pioneers such as Hallen and Schelkunoff[73-77]) focused on deriving analytical expressions for the current distribution on an antenna.

In their work, the only geometry to which an analytical solution is available (to our knowledge) is the simple dipole antenna. Analytical expressions are available as series expansions in the parameter d/l, where d is the diameter and l the length. Virtually all of modern antenna theory takes as its canonical example the characteristics of a dipole antenna in the limit d/l goes to zero.

Now, with the advent of cm long carbon nanotubes, it is possible to fabricate conducting wires with unprecedented aspect ratios of order  $10^7$ . This has led us to propose a nanotube antenna, shown in Fig. 14. At first sight, it would seem that this new system would be the closest physical realization to a dipole antenna (in the sense that d/l is small) mankind has ever manufactured. However, this is not the case, as we elaborate on below.

In original theoretical work on dipole antennas, it was assumed that the dipole radius was larger than the skin depth, *and* that the resistive losses were low enough to be neglected in determining the current distribution on the antenna. Both of these assumptions break down for nanotube antennas. Therefore, the original theory and hence the only analytical theory breaks

down in the limit d/l becomes sufficiently small.

In a one-dimensional conductor such as a nanotube, the concept of skin-depth is almost meaningless, since the electrons are only free to move along the length of the wire, and not in the transverse direction. Therefore the current distribution is effectively one-dimensional. In addition to the electron transport occurring in only one dimension, we also have two more important effects: large resistance, and large inductance.

These effects give rise to very different behavior for a nanotube antenna, as compared to a classical antenna. The main difference is the current distribution is periodic with a wavelength about 100 times smaller than the free space wavelength for a given temporal frequency. The comparison of the current distribution on a nanotube dipole antenna to a classical dipole antenna is shown in Fig. 15 below (from Ref.[70], with permission). It is clear that the current distributions are dramatically different. Our work has been further developed numerically by Hanson[71].

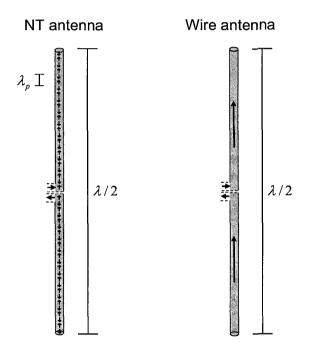


Fig 15: Current distribution on a nanotube antenna vs. classical wire antenna.  $\lambda$  is the free space wavelength (set by the frequency), and  $\lambda_p$  is the wavelength of the current distribution on a nanotube, which is typically about 100 times smaller than the free space wavelength, from [70].

Our calculations[70] show that the efficiency of a classical nanotube dipole antenna is poor, due to resistive losses. However, we have proposed that possibly other geometries (to be

determined) could and should be investigated that take advantage of the unique materials and electronic properties of carbon nanotubes. An important issue is that of impedance matching the antenna to any generator, which will depend on the source impedance of the generator.

A more general theory of nanotube "antennas" which applies even in the optical frequency range to scattering experiments[78] has been developed in [79-84]. The application of the concept of antenna is really not limited just to the RF frequency range. However, much theoretical and experimental work remains to be done to truly understand and utilize the concepts in engineering applications.

#### 13. Conclusions

In this paper, we have reviewed the potential applications of single-walled carbon nanotubes in three areas: passives (interconnects), actives (transistors), and antennas. In the area of actives, potential applications include transistors for RF and microwave amplifiers, mixers, detectors, and filters. While the experimental and theoretical state-of-the art is clearly in its infancy, the promise for high frequency electronics is great, and progress is extremely fast. It is not a stretch to predict that nanotubes will find applications in high frequency electronic systems sometime in the future.

#### 14. Acknowledgements

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# NANOTUBES AND NANOWIRES

he field of nanotubes and nanowires is evolving at a rapid pace, with many potential applications in electronics, optics, and sensors, to name a few. In this book, various prominent researchers summarize our current understanding of these new materials systems, as well as some of these potential applications. A snapshot of the state-of-the-art in the field of nanowires and nanotubes, the contributions give an instructive mix of experimental, theoretical, and visionary material to give the reader an indication of where the field is now, and where it is going.

With several points of view represented, including academic theoreticians, academic experimental device engineers, and industry researchers from well-known semiconductor companies, *Nanotubes and Nanowires* is an essential source of reference for physicists, chemists, materials scientists, and graduate students interested in keeping abreast of the latest developments in nanotechnology.

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