FABRICATION AND MEASUREMENT OF ALUMINUM AND CARBON NANOTUBE SINGLE ELECTRON TRANSISTORS FOR RADIO FREQUENCY APPLICATIONS

A Thesis

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by

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CHAPTER 1

INTRODUCTION

The pace of conventional field effect transistors (FET's) scaling has made the devices more difficult and costly to fabricate. In order to continue the miniaturization of circuit elements down to the nanometer scale, researchers are investigating several alternatives to the transistor for ultra-dense circuitry, including the single-electron charging effect. Among the various kinds of single-electron devices, the single-electron transistor (SET), whose operation is based on the tunneling phenomena and Coulomb blockade effect, is perhaps the most important device in this field.

Figure 1.1 gives the schematic of an SET: a conductive island is connected to two lead electrodes (source and drain) through small tunnel junctions, and a gate electrode is capacitively coupled the island. The electrostatic potential of the island electrode can be changed by the modulation of the gate voltage, and thus controls the conductance of the SET. The island is normally referred as "dot" due to its small size. It can be metallic or semiconducting depending on the material forming the island.

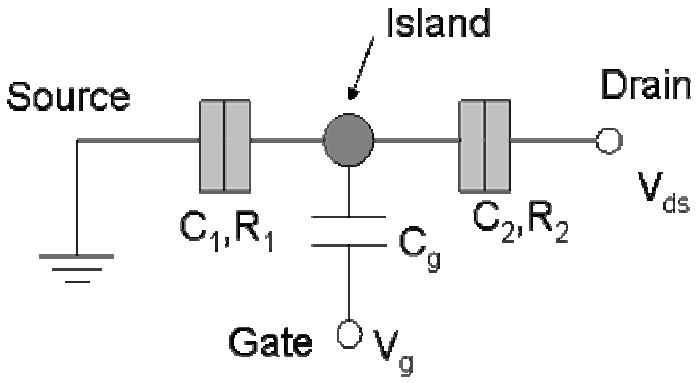


Figure 1.1 Schematic of single electron transistor, consisting of two tunneling junctions connected in series with a small conductive island in between. C_1, C_2 are the capacitance of the tunneling barriers and R_1, R_2 are the resistances. C_g is the coupling capacitance of the gate to the island.

1.1 Single Electron Tunneling

Tunneling by single electrons is the key operational mechanism of Coulomb blockade devices. The single-electron tunneling mechanism, which utilizes the charging energy in a 3-dimensionally confined structure (0D system) such as a quantum dot between adjacent double barriers, was first studied in solids in 1951 by Gorter [1], and later by Giaever and Zeller in 1968 [2], and Lambe and Jaklevic in 1969 [3]. These pioneering experiments investigated transport through thin films consisting of small grains. But because of the random nature of tunneling those systems were uncontrollable and not very useful for studying charging effects. With the development of nanofabrication techniques since the 1970's, new technological control, together with theoretical predictions by Likharev [4] and Mullen *et al.* [5], made it possible to fabricate and study reproducible single

charge tunneling devices. The first clear demonstration of Coulomb blockade oscillations based on controlled single-electron tunneling was performed by Fulton and Dolan in 1987 [13] in an aluminum structure. After these early experiments in metallic junctions, single-electron tunneling phenomenon in semiconductors was first reported by Scott-Thomas *et al*. in 1989 [6].

The orthodox theory developed by Kulik and Shekhter [7] is a clear, effective description of single-electron tunneling. The theory is based on the following major assumptions [8]:

1. The electron energy spectrum is continuous in the source and drain conductors. The number of electrons is quantized only on the island.
2. The time t for electron tunneling through the barrier is assumed to be negligibly small in comparison with other time scales. Where $t = R_j C_j \sim 10^{-10}$ sec and R_j, C_j are the tunneling junction resistance and the capacitance.
3. Coherent quantum processes consisting of several simultaneous tunneling events (co-tunneling) are ignored.

In the orthodox theory of single electron tunneling, tunneling of each electron is an isolated random event and the net charge on the island changes by the charge of exactly one electron (e). The tunneling probability Γ depends solely on the reduction of the free (electrostatic) energy of the system (ΔW) as a result of this

tunneling event [8]:

$$\Gamma(\Delta W)=\frac{\Delta W}{e^2 R_T}\left[1-\exp\left(\frac{-\Delta W}{k_B T}\right)\right]^{-1} \tag{1.1}$$

$$\Delta W = e(V_i - V_f)/2 \tag{1.2}$$

where V_i and V_f are voltage drops across the barrier before and after the tunneling event, respectively.

$$T \Rightarrow 0 \rightarrow \Gamma(\Delta W)=\begin{cases} 0 & \Delta W \le 0 \\ \Delta W/\left(e^2 R_T\right) & \Delta W > 0 \end{cases} \tag{1.3}$$

With known tunneling probability Γ, the tunneling current can be calculated by the simple function.

$$J = -n v_{th} e \Gamma \tag{1.4}$$

1.2 Coulomb Blockade

In single-electron transistors, if an island is small enough, with no or very small applied bias, the energy required to charge the island by an additional electron exceeds the available energy from thermal excitation or applied bias. In this case, no electron tunnel onto the island and no current flows. This so-called Coulomb blockade phenomenon depends on the electrostatic energy necessary to add an extra electron onto the island, which is the charging energy E_C.

$$E_C = \frac{e^2}{2C_\Sigma} \tag{1.5}$$

where e is the charge of one electron and $C_\Sigma = C_1 + C_2 + C_0 + C_g$ is the total

capacitance related to the island: C_1, C_2 are the junction capacitances, C_0 is the self capacitance of the island and C_g is the gate coupling capacitance.

When the charging energy is greater than the thermal energy (k_BT), single electron charging effects will not be smeared out by thermal fluctuations and we can measure discrete electron transfer:

$$E_C = \frac{e^2}{2C_\Sigma} >> k_BT \tag{1.6}$$

Another condition for observing single electron charging effects is the resistance R_T of all the tunnel barriers of the system has to be much higher than the quantum unit of resistance R_Q. This ensures the electron be localized inside the island at any instant.

$$R_T >> R_Q = h/e^2 = 25.8k\Omega \tag{1.7}$$

The total capacitance of an SET is normally very small, less than 1 fF (10^{-15} F), so the charging energy is greater than the thermal energy only for temperatures of a few Kelvin or less. At such temperatures, electron transport through the island is determined by Coulomb charging. When the energy difference between the island and the source or drain is larger than the charging energy E_C, an electron can tunnel to or out of the island, figure 1.2 (a), (b), (c) shows the sequence of a single electron tunneling through the barriers. In this case, the device is conducting. If the energy difference on either side of the barriers is less than E_C, the number of electrons on the island is fixed and the device is in Coulomb blockade state (figure 1.2 (d), (e)).

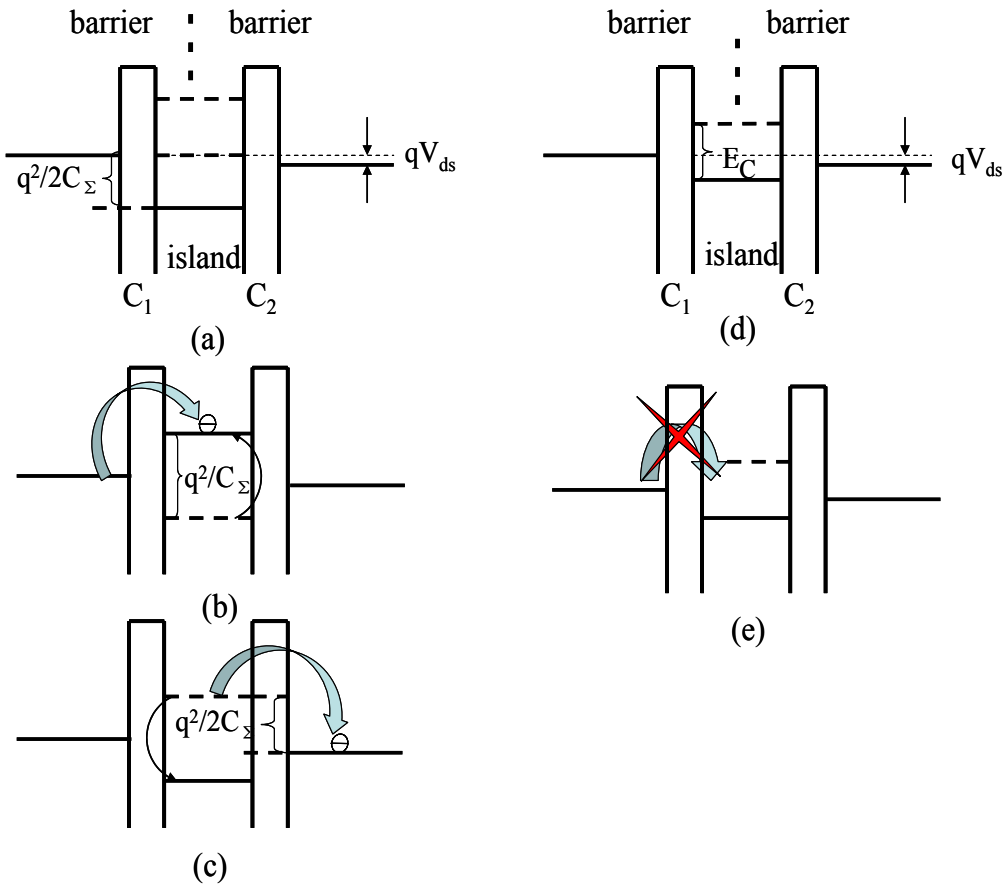


Figure 1.2 Tunneling dynamic for SETs. (a), (b), (c) shows the conducting state; (d), (e) shows the blocked state.

An SET switches from the off-state (Coulomb blockade) to the on-state (conducting) when half an electron is added to the gate. This is orders of magnitude less charge than is necessary at the gate of a field-effect transistor to switch it from off to on. The periodic dependence of conductance vs. V_g which is often called Coulomb blockade oscillations (figure 1.3) is due to the quantization of the number of electrons on the island. By applying the gate voltage, the energy potential of the island can be changed and thus the number of electrons on it can be changed one by one. The valleys of the oscillations mean there is no current

flow through the island. One period of gate voltage change ΔV_g correspond to the addition of one electron onto the island. If the gate coupling capacitance is C_g, then:

$$C_g \Delta V_g = e \tag{1.8}$$

The finite width of the conductance peaks are caused by thermal excitation. The width of the peaks shrinks with decreasing temperature. At lower temperature, the oscillations are more like δ functions.

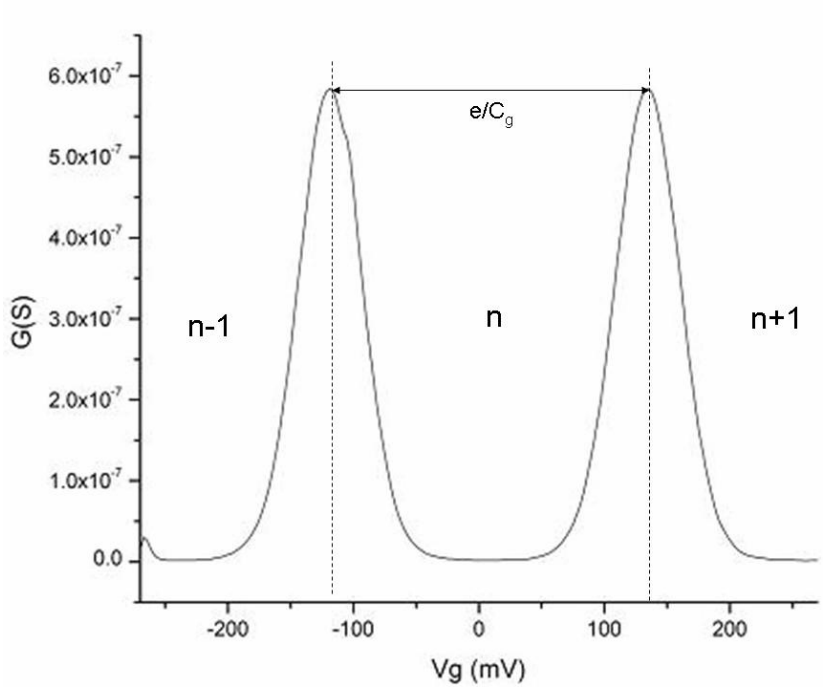
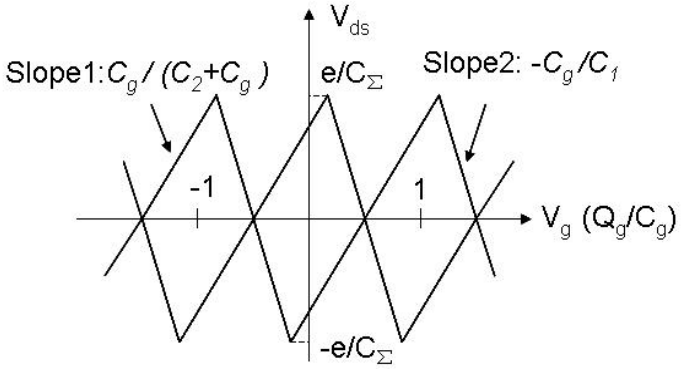
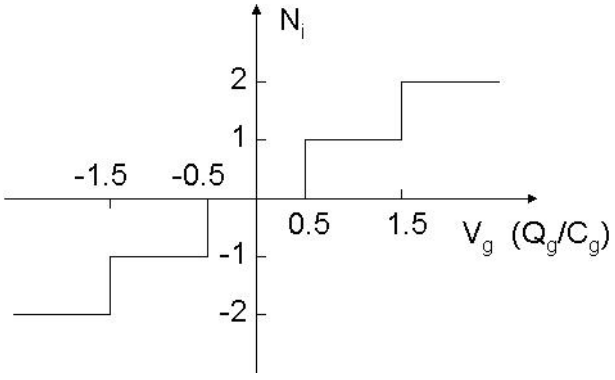


Figure 1.3 Coulomb blockade oscillations. From one valley to the next valley there has been one additional electron added to the island.

Figure 1.4 (a) shows the Coulomb blockade charging diagram. The areas of the diamond shapes are where the conductance is blocked. C_1, C_2 are the junction capacitances and C_g is the gate coupling capacitance to the island. With the device staying in the Coulomb blockade state ($-\frac{e}{2C_\Sigma} < V_{ds} < \frac{e}{2C_\Sigma}$), the excess electrons on the island are introduced by changing the gate voltage V_g (figure 1.4 (b)).



(a)



(b)

Figure 1.4 (a) Coulomb diamond; conductance is blocked inside the rhombus regions. The rhombus has slopes of $-C_g/(C_g+C_2)$ on one side and C_g/C_1 on the other side. (b) Number of excess electrons on the island which is introduced by the gate voltage.

1.3 Charge Sensitivity

Single-electron transistors are the most sensitive and fast charge sensing devices available.

The charge sensitivity can be calculated from the measured single-to-noise ratio (SNR) and the input signal. For an input signal with amplitude Δq (rms) in unit of e, the sensitivity δq is given by [9]:

$$\delta q = \frac{\Delta q}{\sqrt{B} \cdot 10^{SNR/20}} \quad (e/\sqrt{Hz}) \tag{1.9}$$

where B is the measurement bandwidth.

Then the energy sensitivity is given by:

$$\delta E = (\delta q)^2 / (2C_{\Sigma}) \tag{1.10}$$

The low-frequency charge sensitivity ($< 10^{-5}\ e/\sqrt{Hz}$) of the SET is limited by *1/f* noise due to the motion of background charge. Although this can be improved as the frequency increased, SET performance is still limited by the thermal/shot noise of the SET. In order to display a strong Coulomb blockade and a sharp on-set current, (or suppress quantum fluctuation) each junction of the SET must be of the order of the quantum resistance (R_Q=25.8 kΩ) which leads to a large output resistance of the SET ($R_{SET} \geq$ 50 kΩ), given the parasitic capacitance ($C_p \geq$ 1 pF) of the cabling to the room temperature measurement devices, the bandwidth is limited by the corresponding $R_{SET}C_p$ time constant to a few kHz ($B \leq 1/2\pi R_{SET}C_p$) although the intrinsic limit of the SET speed is determined by R_jC_j (C_j is the junction capacitance) time constant which can be greater than 10 GHz.

It has been found [11] that the signal to noise ratio (SNR) scales as $SNR \propto \sqrt{e/RC}$, so maintaining a small C can increase the charging energy and a small RC product can improve the ultimate charge sensitivity of the SET.

1.4 Radio-Frequency Single Electron Transistor (RF-SET)

The RF-SET is a new type of SET which is a very fast readout of the charge coupled through the gate capacitor. It can work up to 100 MHz where *1/f* noise can be negligible. Rather than measuring the output current or voltage, the readout of the charge state of RF-SET is done by measuring the damping of a high frequency signal added onto V_{ds} in the time domain. It allows large operating speeds and extremely high charge sensitivity and is more than three orders of magnitude faster than conventional single-electron devices.

The charge sensitivity of RF-SET is limited by the shot noise; it can be an order of magnitude better than conventional SET [12]. A sensitivity of 3.2×10^{-6} $e/\sqrt{Hz}$ has been achieved at 8 MHz for a superconducting RF-SET [9].

1.5 Structure of Thesis

This thesis consists of five chapters. Chapter 2 gives the details on fabrication of Aluminum SETs and a brief discussion of measurement techniques. The measurement results including tunneling resistance control during fabrication and

low temperature measurement of I-V characteristics and Coulomb blockade diagrams will be shown in chapter 3. The measurement setup for RF-SETs will also be discussed. Chapter 4 describes measurements on single-wall carbon nanotubes which also show single electron effects at low temperature. Finally chapter 5 will summarize and describe possible future work.

CHAPTER 2

FABRICATION OF ALUMINUM SINGLE ELECTRON TRANSISTORS

In this chapter, the fabrication techniques used to make the aluminum tunnel junction devices will be described. The procedure includes RCA clean, thermal oxidation, optical lithography, electron beam lithography (EBL), and double-angle evaporation of aluminum. The basic measurement setup will also be discussed.

2.1 Fabrication of Leads and Bonding-pads

The fabrication starts with a plain 4 inch Silicon wafer. Before any further procedure, the contaminants on the surface are chemically removed using RCA (Radio Corporation of America) MOS clean procedure, including 10 minute dips in 1:1:40~50 solution of NH_4OH : H_2O_2 : H_2O and 1:1:40~50 solution of HCL : H_2O_2 :H_2O. Both of the solutions are heated to 70^oC. Followed these dips, the wafers are immersed for 30 seconds in buffered HF. After that, a 350 nm thick SiO_2 layer is thermally grown on the wafer to isolate the devices on top of the oxide from the conducting silicon substrate.

The fabrication steps are shown in figure 2.1. The procedure includes two

optical lithography and metal deposition steps to form the two layers. Since lift-off is used to form the metal patterns, it is important that the photoresist is thicker than the metal deposited. Another important thing is a strong under-cut profile of photoresist after development as shown in figure 2.1 (b).

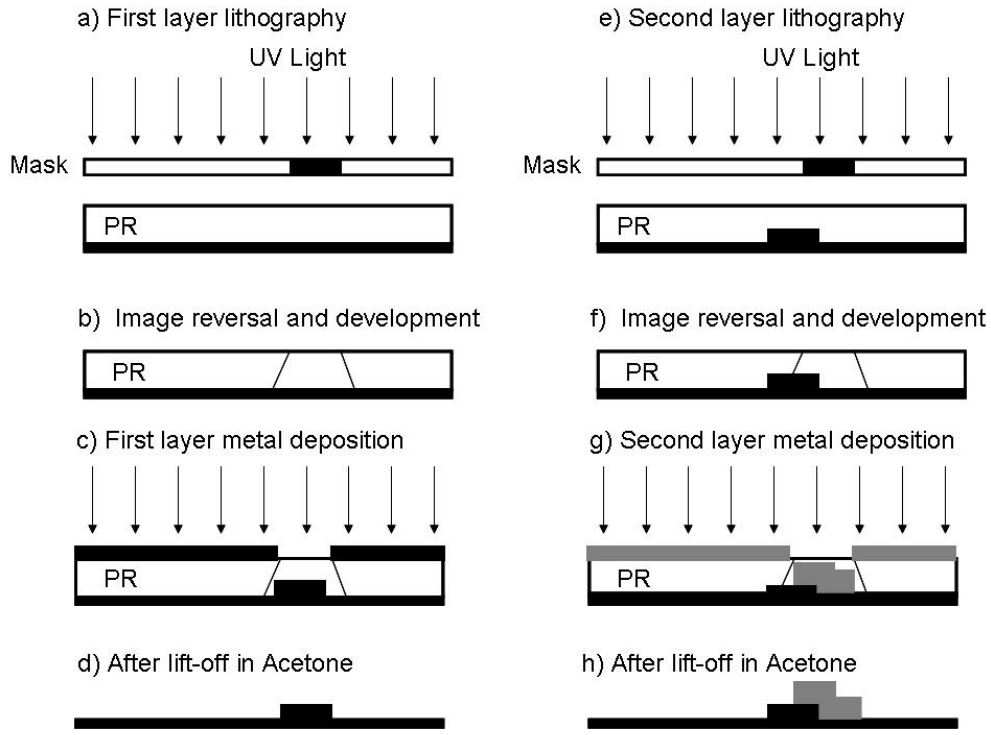


Figure 2.1 Schematic diagram of the photolithography process. The process involves two photolithography steps with subsequent metal evaporation. The image reversal and a good under-cut are important in metal deposition. 5 nm Titanium and 20 nm Platinum are deposited for the first layer, 5 nm Titanium and 200 nm gold for the second layer. A thin layer of Titanium gives a better adhesion between the deposited metal and silicon substrate.

Figure 2.2 shows the finished substrate of the device with two layers of metal. The main purpose of the first platinum layer, which consists of 6 μm wide rectangular pads, is to provide a 250 Å thick transition layer metal between the electron beam metal layer of aluminum (400 Å to 600 Å) and a much thicker

bonding pad metal layer of gold (2000 Å). A thick layer of gold is used to give a better contrast for alignment in electron-beam lithography, and to make bonding easier. In each single die a test structure is included to test the continuity between two metal layers (Figure 2.2 (c)).

Figure 2.2 (d) shows the close-up view of the central region of a single die where electron beam lithography will be done, along with the focus features and alignment marks for EBL which are on the second layer. The 1~2 μm focus features consist of crosses and squares. The size of the four square-shaped EBL alignment marks are 10 μm x 10 μm and the distance between each is 100 μm. These features are on the second layer is because the layer of gold can give a better contrast and brightness in the EBL system, ensuring clear focusing and aligning during the EBL. The area of the central region which is surrounded by the first layer fingers is 65 μm by 65 μm.

If the photoresist under-cut is not good, it will result in metal curling on the edge, which is often called “rabbit ears” or “wings”. Figure 2.3 shows a schematic illustration of formation of rabbit ears due to inadequate photoresist under-cut. Figure 2.4 shows some SEM images examples of edge wings. The curling edge often results in broken metallization in the next metal layer around the step region, giving an open circuit (Figure 2.4 (b)).

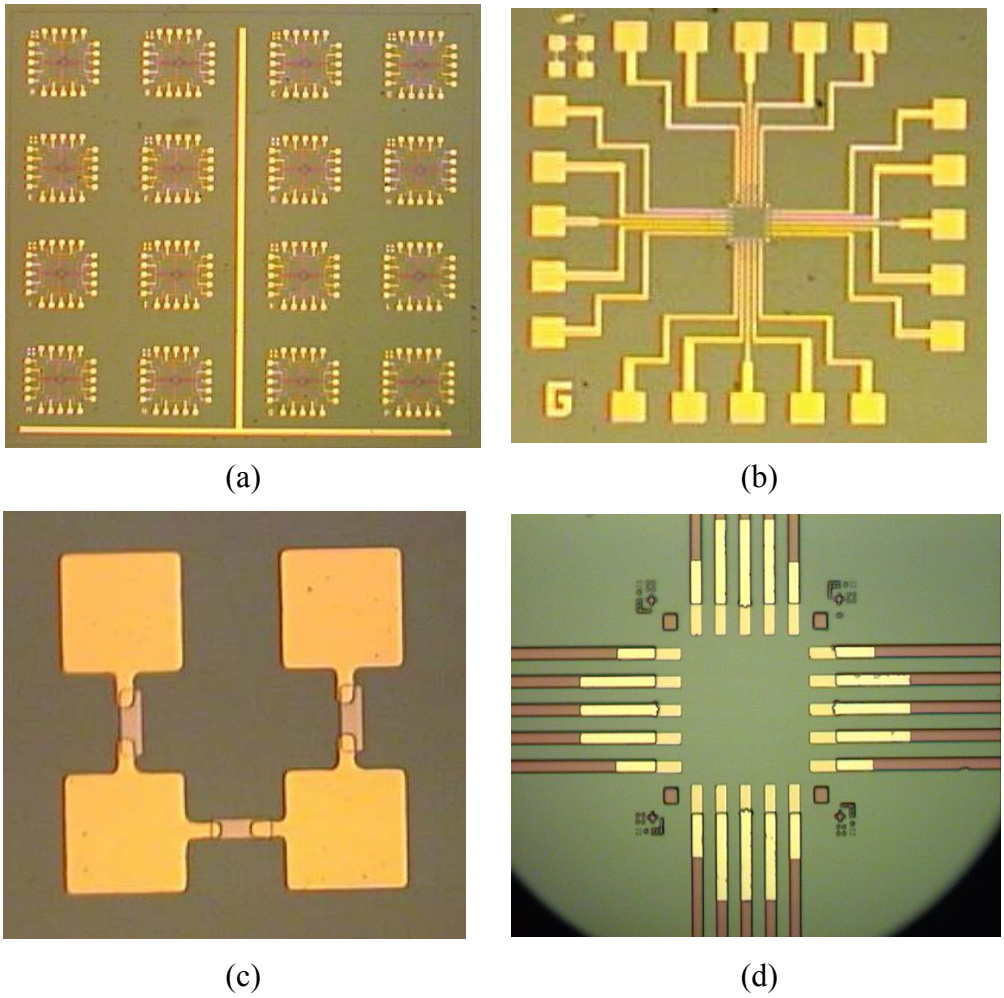


Figure 2.2 Substrate of SET with two layers of metal. (a) Pattern of one exposure which has sixteen 20-pin die. (b) Single die of the substrate. (c) Test structure for testing the continuity between two metal layers after fabrication. (d) Central region of each die showing the two layers of metal and alignment marks for EBL.

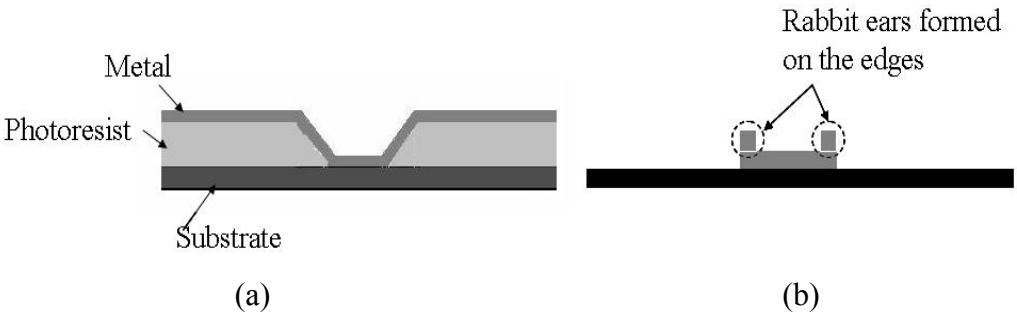
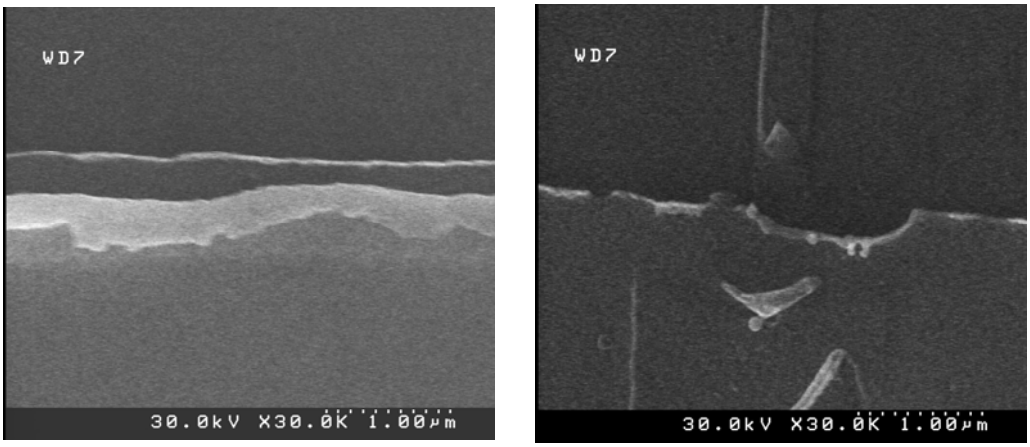


Figure 2.3 Schematic illustrating formation of rabbit ears. (a) Instead of under-cut, the photoresist gives a positive slope. (b) Deposited metal on the edges curls up during lift-off, forming rabbit ears.



(a) (b)

Figure 2.4 (a) "Rabbit ears" forms on the edge during lift-off of a bad under-cut. (b) A broken wire on top layer due to the curling of the bottom metal layer.

Normally there will be some photoresist residue left on the substrate after lift-off. This will lead to a bad contact between metal layers and give a low yield. Piranha etch is used to get rid of this residue. The standard piranha solution is a 3:1 mixture of sulfuric acid (H_2SO_4) with hydrogen peroxide (H_2O_2). It is self-heating and self-starting as soon as hydrogen peroxide is added to the sulfuric acid. A 35 second dip followed by 30 sec IPA rinsing is generally enough to remove the resist residue.

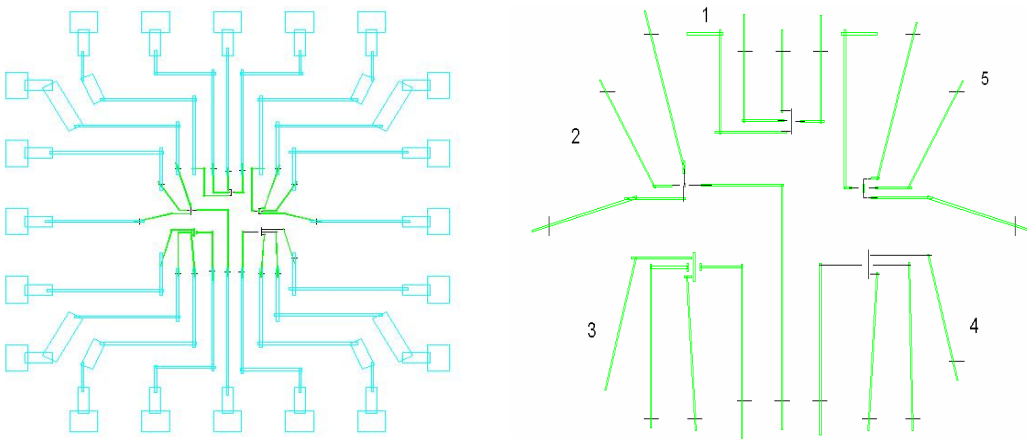
2.2 SET Fabrication

2.2.1 Electron Beam Lithography (EBL)

The fine features of the single electron transistor are fabricated by electron beam lithography. The lithography is done in Amray 1400 scanning electron

microscope EBL system. It uses a tungsten filament electron source and the electron beam is accelerated by a large voltage of 40 to 50 kV with a typical beam current of 10 pA.

The lithography pattern is designed using the NPGS (Nanometer Pattern Generation System) software. Figure 2.5 shows the lithography pattern. The software also controls the alignment and the operation of the beam blanker during lithography, as well as the exposure dose and center to center distance between pixels. All the features are made as a combination of closely spaced dots or pixels. Exposure time of each dot is determined by the electron dose. The center to center distance between dots contributes to the line width. At a working distance of 10 mm, the typical line dose of our lithography is 3.5 nC/cm and area dose is 400 $\mu C/cm^2$. The center-to-center pixel distances for line and area regions are 41.9Å and 209.4Å respectively.

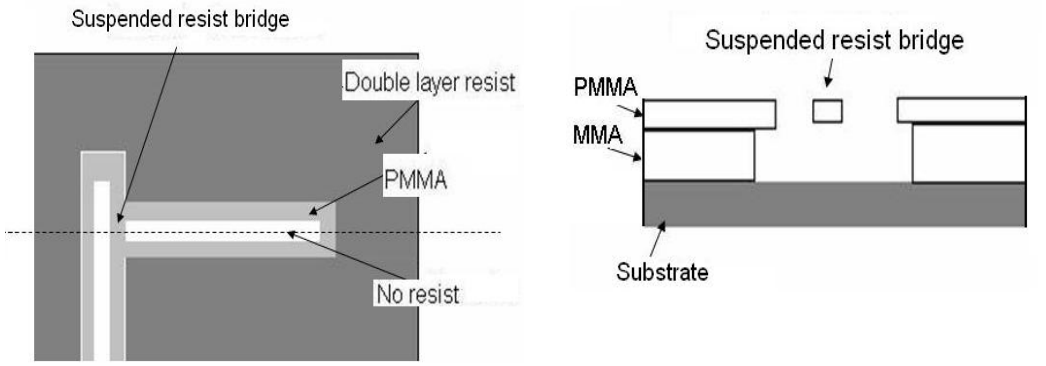


(a) (b)

Figure 2.5 (a) NPGS pattern of SETs, (b) central part of the pattern, showing five different SET designs.

Double layer resists are used with different electron beam sensitivity. The first layer is 9% MMA (methyl methacrylate) by weight in methacrylic acid (MAA) spun at 4000 rpm for 30 sec and baked at 170°C for 3 min, while the second layer is 2% by weight 950,000 amu polymethylmethacrylate (PMMA) in chlorobenzene spun at 4000 rpm for 30 sec and baked at 170°C for 2 min. The total thickness of the resists is around 450 nm.

Since MMA is more sensitive to the electron beam, it leads to a large under-cut after development for easy lift-off. Figure 2.6 shows a schematic of the resists after e-beam exposure and development. Due to the higher sensitivity of MMA, the large under-cut forms a suspended PMMA resist bridge. This is used to form the junctions.



(a) (b)

Figure 2.6 Schematic for double-angle evaporation steps in forming junctions. (a) Top view after development. (b) Cross section view along dashed line. Due to the different beam sensitivity of MMA and PMMA, a suspended resist bridge is formed.

2.2.2. Double Angle Evaporation

The experiment of making aluminum tunneling junctions is first demonstrated by Fulton and Dolan in 1987 [13]. With two metal layers deposited at different angles, an overlap of these two layers can be achieved in a small region. An intermediate *in situ* oxidation is performed between the two depositions, thus there is an oxide layer between two metal layers which forms the Al/ AlO_x/ Al tunnel junction.

The angle of evaporation needed is determined by the separation of the lines forming the junction and the thickness of the resist. The distance between the lines is set to be 100 nm and the thickness of double layer resist is normally 450 nm, so the angle used in our fabrication process is ±6.5º.The evaporation angle is critical since if it is too small, there will be no overlapping junctions, and if it is too large, the metal will be deposited on the resist sidewall. After lift-off, any metal on the sidewalls may dislodge and drop on our pattern, sometimes shorting the circuit.

The evaporation is done using 99.999% Aluminum in the Veeco thermal evaporator, which has a variable angle sample stage. The stage is set directly above the aluminum source. 3-4 small pellets of aluminum are put in a twisted tungsten basket. A high current is applied through the basket which heats it up, melts the aluminum pellets and makes aluminum evaporate. At a base pressure of $5x10^{-7}$ torr, the first layer of aluminum is deposited at an angle of -6.5º for a thickness of 200-250 Å, then 50 - 70 mTorr oxygen gas of 99.9999% purity is let

into the evaporation chamber for 8 to 15 min to oxidize the aluminum. After that a thicker layer (400~500 Å) of aluminum is deposited at an angle of +6.5º to get a good coverage of the first layer. Former experimenters found that the evaporation of aluminum must be performed at a high rate (> 25 Å) to yield a good quality film with small grain size. This is particularly important for our devices since the junction overlap area is usually less than 100 nm x 100 nm. Figure 2.7 shows the steps of the double angle deposition and junction formation in more details. Figure 2.8 is the SEM images of final devices.

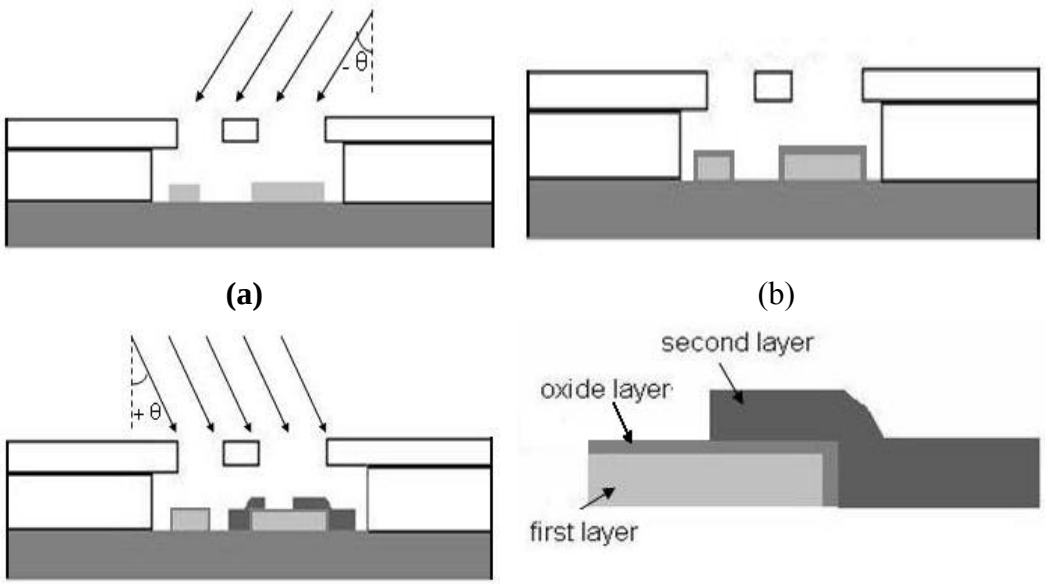
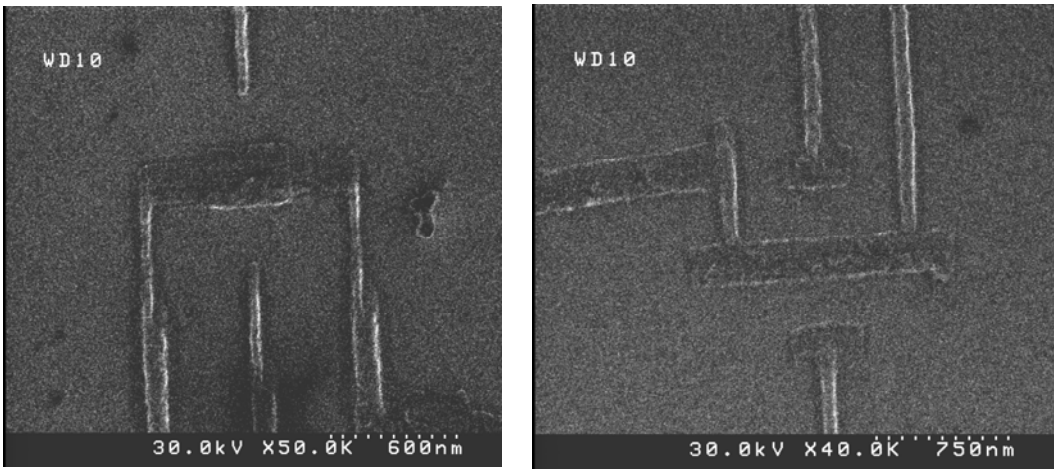


Figure 2.7 Schematic for double-angle evaporation steps in forming junctions. (a) First aluminum evaporation, (b) *in-situ* oxidation, (c) Second aluminum evaporation, (d) After lift-off in acetone. Al/ AlO_x/ Al tunneling junction formed at the overlap.



(a) (b)

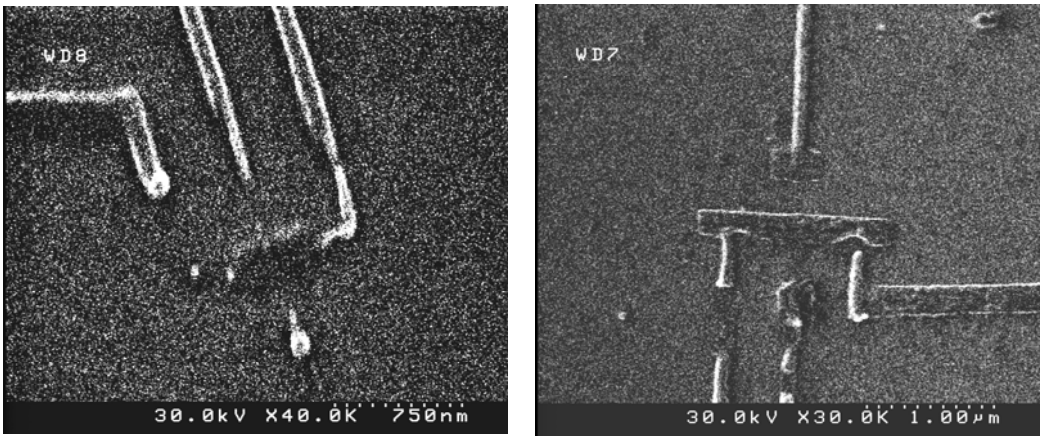
Figure 2.8 SEM micrographs of metal-island SETs fabricated using the double-angle evaporation technology. The single line width is around 80 nm.

The lift-off in acetone often leaves some polymer residue around the deposited aluminum. This residue does not cause any problem during measurements, but makes it difficult to image the sample with SEM. In order to get a much clearer image, the residue is removed by rinsing the sample in Acryl Strip (99% acetic acid) for 20 min or more.

2.3 Fabrication Issues

Single electron transistors are extremely charge-sensitive devices. External electrostatic discharge will easily melt the junctions and destroy the devices. Proper handling is important when fabricating SETs. The samples are carried in conductive, anti-static carriers. A grounding strap and anti-static gloves must be worn while handling the devices. Proper grounding of the stages and pins is

necessary when testing and bonding the devices. Figure 2.9 shows examples of SETs that have been destroyed by electrostatic discharge. It can be seen that not only are the junctions melted, but the leads and the islands are also broken, leading to open circuits.



(a) (b)

Figure 2.9 Examples of SET devices destroyed by electrostatic discharge. The junctions were melted by the discharge.

Misalignment during electron beam lithography is another problem encountered. There are many reasons for misalignment, the most common of which is mechanical drifting of the stage during lithography. Figure 2.10 gives an AFM image of one of the devices. Due to the stage drifting, the lines are shifted and lead to an open circuit.

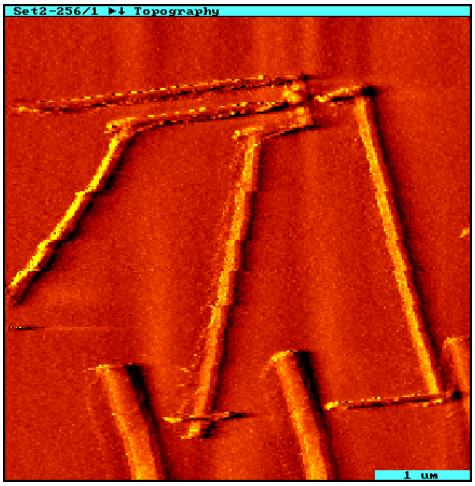


Figure 2.10 AFM image of an SET. Due to drifting during EBL, the wires didn't connect to each other, leading to an open circuit.

2.4 Measurement Setup

Immediately after the fabrication of the device, a room temperature I-V_{ds} measurement is done on a probe station controlled by DAAS software (Data Acquisition and Analysis System) with a sweeping of V_{ds} from -2 mV to 2 mV. The equipment consists of a Micromanipulator 8065 and Keithley 236 Source Measurement Unit. The resistance of the devices typically varies from several kΩ to a few MΩ. After testing at room temperature, the device is bonded to a 20-pin ceramic chip package using the West Bond 7400 wedge bonder.

The low temperature measurements are performed using ^{4}He dipper (4.2K) and Oxford Instruments Heliox ^{3}He cryostat with a base temperature around 300 mK. The package is loaded into a 20-pin socket located on the bottom of the cold finger of the fridge insert or 48-pin socket mounted at a dipper. As a precaution

against electrostatic discharge, all the pins on the socket are grounded. Since aluminum becomes superconducting around 1.2 Kelvin, a 1T magnetic field is applied to suppress the superconductivity and bring the device back to the normal state.

All the measurements are based on the lock-in technique using Stanford Research 830 Lock-in Amplifiers. Figure 2.11 shows a simplified schematic diagram of our measurement setup. The source lead is virtually grounded and a small AC excitation signal, typically 100 μV for better SNR, is applied to the other (drain) lead.

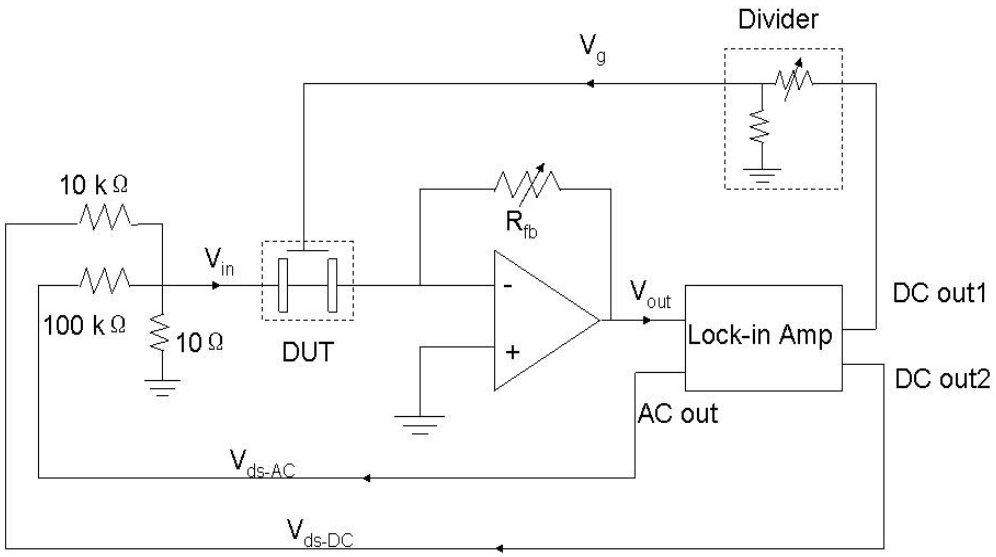


Figure 2.11 Schematic diagram of measurement setup. The feedback resistance R_{fb} can be changed from 100K Ohms to 10M Ohms. The output voltage of the pre-amp is read by the Lock-in Amplifier.

The differential conductance (dI/dV) of the device is measured through an I-V converter. Due to the negative feedback in the pre-amp, the conductance and the output voltage are related as:

$$V_{in} \times G_{SET} = -V_{out} \times G_{fb} \tag{2.1}$$

So

$$G_{SET} = -\frac{G_{fb}}{V_{in}} V_{out} \tag{2.2}$$

The output voltage of the I-V converter is fed to the input of the lock-in amplifier. The 180º phase change from the pre-amp is taken into account when assigning values to the Lock-in output. The I-V converter is powered by battery in order to suppress the formation of ground loops. The DC source-drain bias and gate voltage are provided by the built-in DACs of the lock-in amplifier.

The data is collected by data acquisition software "DAAS" written by Dr. Greg Bazan. This program controls the gate and source drain DC voltages, and acquires data from lock-in output.

CHAPTER 3

MEASUREMENT OF ALUMINUM SINGLE ELECTRON TRANSISTORS

3.1 Oxidation vs. Tunneling Resistance

The *in-situ* oxidation of the first layer aluminum is important because it forms the tunneling barriers for the device and the tunneling capacitance (C_T) and resistance (R_T) are sensitive to the barrier thickness. For the future RF-SET measurements, a low resistance is needed for better resolution and at the same time a relatively high charging energy should be maintained also. Since $E_C=e^2/2C$, there will be an optimized point where both resistance and capacitance are suitable for RF measurements. As mentioned in Chapter 1, another reason for controlling R_T and C_T is for better charge sensitivity since $\delta q \propto 10^{\sqrt{RC}}$.

Taken as a parallel plate capacitor, the junction capacitance is inversely proportional to the oxide layer thickness since $C = \varepsilon \frac{S}{d}$, where d is the thickness of the oxide layer and S is the overlap area. The tunnel resistance can be calculated from $R_T = \frac{V}{e\Gamma}$, where V is the voltage drop across the tunneling barrier and Γ is the tunneling probability which is proportional to *exp(-d)*, thus R_T is proportional to *exp(d)*. In principle, the oxide layer thickness can be controlled by controlling the oxidation time and pressure, so the resistance and capacitance of the device can be

determined.

The oxidation conditions were explored by fixing the oxidation time at 10 minutes and changing the oxidation pressure. Table 3.1 and figure 3.2 (a) give the measured SET resistances obtained at different oxidation pressures, and figure 3.2 (b) shows the distribution of the resistances. The resistances are source-drain resistances which are measured on the probe station at room temperature right after fabrication. We can clearly see that the resistances show a strong dependence on the oxidation pressure. So it is possible to control the SET resistance by controlling the oxidation pressure.

TABLE 3.1

EXPERIMENTAL DATA OF SET RESISTANCES AT DIFFERENT OXIDATION PRESSURE FOR 10 MINUTES OXIDATION

	Average resistance (Ohms)	Standard deviation (Ohms)	Standard error (Ohms)
P=60 mTorr	4.37×10^5	6.15×10^5	2.05×10^5
P=50 mTorr	5.79×10^5	3.64×10^5	1.29×10^5
P=30 mTorr	3.05×10^5	3.38×10^5	1.19×10^5
P=10 mTorr	3.17×10^4	1.80×10^4	6.79×10^3

The standard deviation is calculated as:

$$SD = \sqrt{Var} \tag{3.1}$$

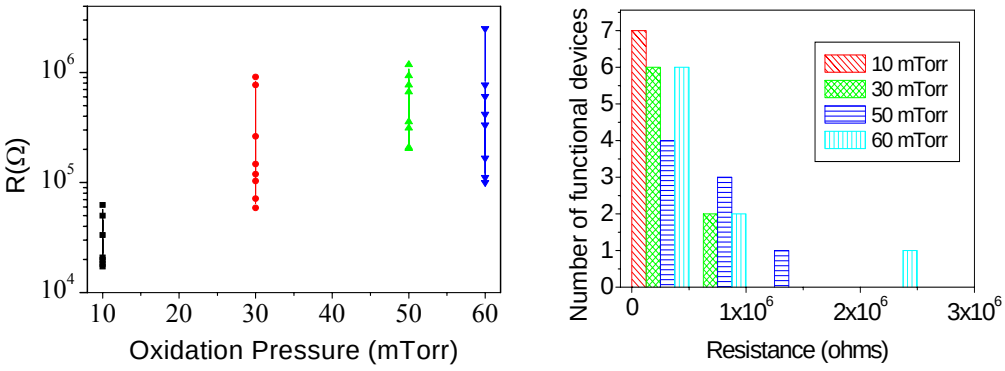
Where

$$Var = \frac{1}{n-1}\sum_{i=1}^{n}(X_i - \overline{X})^2 \tag{3.2}$$

n is the number of points and $\overline{X}$ is the average value.

The standard error is calculated as:

$$SE = \frac{SD}{\sqrt{n}} \tag{3.3}$$



(a) (b)

Figure 3.1 (a) SET resistance at different oxidation pressure. Oxidation time is kept the same at 10 minutes. (b) Resistance distribution of each pressure. Certain oxidation pressure results the SET resistances in certain range, so the resistance is controllable.

3.2 Thermometer Behavior of SET

In the high temperature region where the charging energy $E_C << k_BT$, the SET behaves like a thermometer. The full width at half maximum (FWHM) of source-drain bias voltage of the conductance drop $V_{1/2}$ divided by temperature is a constant number. It does not depend on the Coulomb blockade [14]. Figure 3.3

shows that $V_{1/2}$ is the same for $E_C = 0.25k_BT$ or $E_C = 0.05k_BT$ at the same temperature. G_T is the conductance at the valley. $\Delta G/G_T$ is the normalized relative change of conductance.

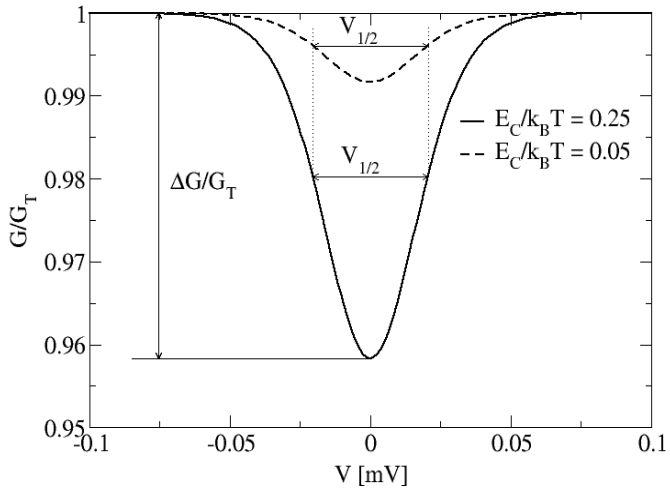


Figure 3.2 When E_C << kT, the full width bias voltage at half maximum of the conductance drop $V_{1/2}$ does not depend on the Coulomb blockade [14].

Theoretically for symmetric multiple junctions in series, the equation is:

$$\frac{eV_{1/2}}{Nk_BT} = 5.439 \tag{3.4}$$

where N is the number of tunnel junctions in the linear array.

By definition, a primary thermometer is one whose equation of state can be written down without the introduction of unknown, and possibly temperature dependent, constants. In this way, the SET shows a primary thermometer quality:

$$V_{1/2} = \frac{5.439Nk_BT}{e} \tag{3.5}$$

J. P. Pekola et al. in 1994 experimentally demonstrated this result. They also showed that the FWHM of conductance peaks scales with *N/2*. In addition to $V_{1/2}$ being proportional to *T*, the relative change of conductance ($\frac{\Delta G}{G}$) is inversely proportional to *T* [15], which gives a secondary thermometer (one which needs to be calibrated) based on known temperature dependence of E_c:

$$\frac{\Delta G}{G} = \frac{E_c}{6k_B T} \tag{3.6}$$

where $E_c = \frac{(N-1)e^2}{NC_\Sigma}$ is the charging energy of *N* tunneling junctions in an array.

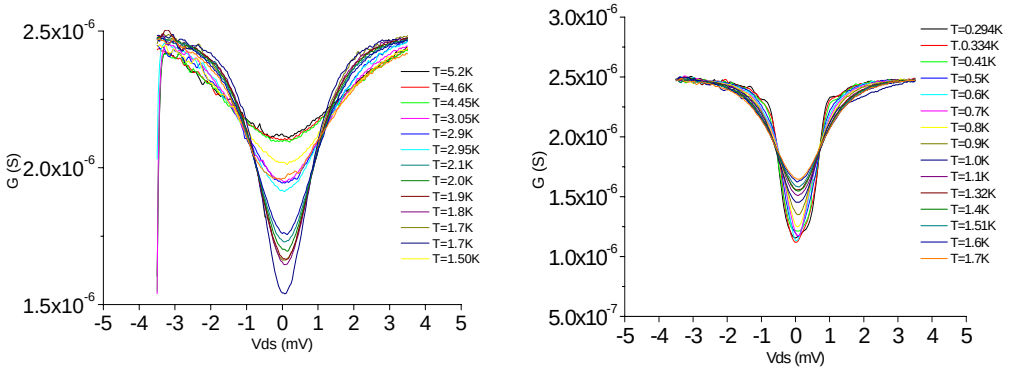
When the temperature is not very high, i.e. when $E_C << k_B T$ does not hold, there is a low temperature correction to the basic result $\frac{eV_{1/2}}{Nk_B T} = 5.439$ [14]:

$$T = \frac{eV_{1/2}}{5.439Nk_B}(1 + 0.392\frac{\Delta G}{G})^{-1} \tag{3.7}$$

In the $E_C << k_B T$ regime, the $V_{1/2}$ and $\Delta G/G$ show linear temperature dependences. In the region where $E_C \leq k_B T$, the temperature dependence follows the modified thermometer formula (3.7). When $E_C > k_B T$, the Coulomb blockade dominates, also the change of the conductance is mainly effected by the change of the background charge rather than the temperature dependence.

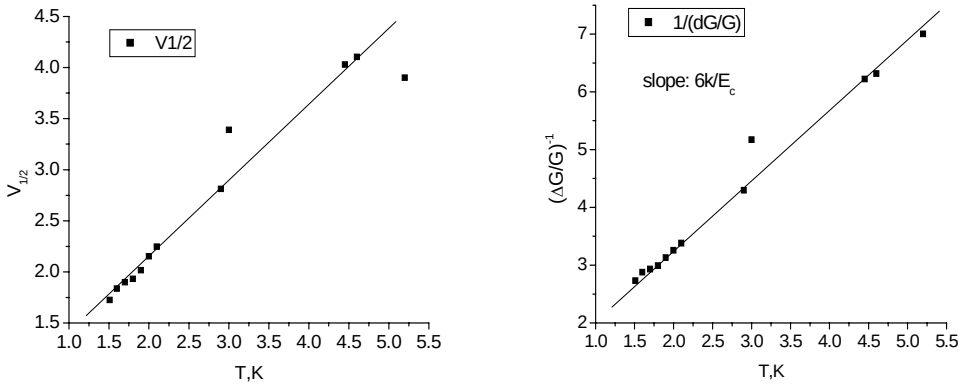
The thermometer behavior of SET is very important because it gives a good estimate of the real temperature of the devices. Figure 3.3 and figure 3.4 are the experimental results. The temperature dependence of *G* vs. V_{ds} plots is shown in figure 3.3. For temperatures from 300 mK to 5.5 K, the conductance peak

becomes deeper and the FWHM of the conductance becomes wider. The linear temperature dependence of $V_{1/2}$ and $\Delta G/G$ is shown in figure 3.4, which fits the theory of primary thermometer and secondary thermometer behavior of an SET.



(a) (b)

Figure 3.3 Temperature dependence of conductance verses source-drain bias at low temperature region from 300mK to 1.7K (a) and high temperature region from 1.5K to 5.2K (b).



(a) (b)

Figure 3.4 (a) Primary thermometer behavior shown by the temperature dependence of $V_{1/2}$. (b) Secondary thermometer behavior shown by the temperature dependence of $\Delta G/G$.

For two junctions N=2, the formula becomes:

$$\frac{eV_{1/2}}{2k_BT} = 5.439 \tag{3.8}$$

The calculated constant (5.439 in ideal theory) case shows a larger deviation at lower temperature than higher temperature from 300 mK to 1.5 K as shown in figure 3.5 (hollow squares). The flat line is the expected value 5.439. The solid squares show the low temperature correction for the data using formula:

$$\frac{eV_{1/2}}{2k_BT}\left(1+0.392\frac{\Delta G}{G}\right)^{-1} = 5.439 \tag{3.9}$$

It can be seen that the corrected formula provides a better fit to the theoretical constant.

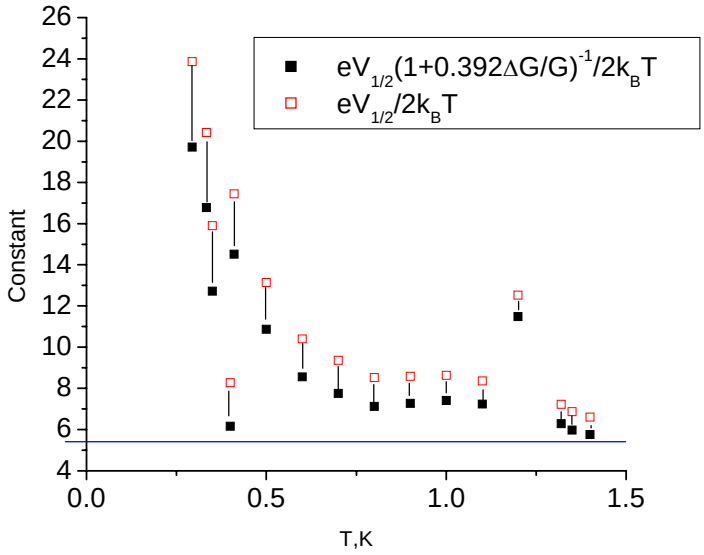
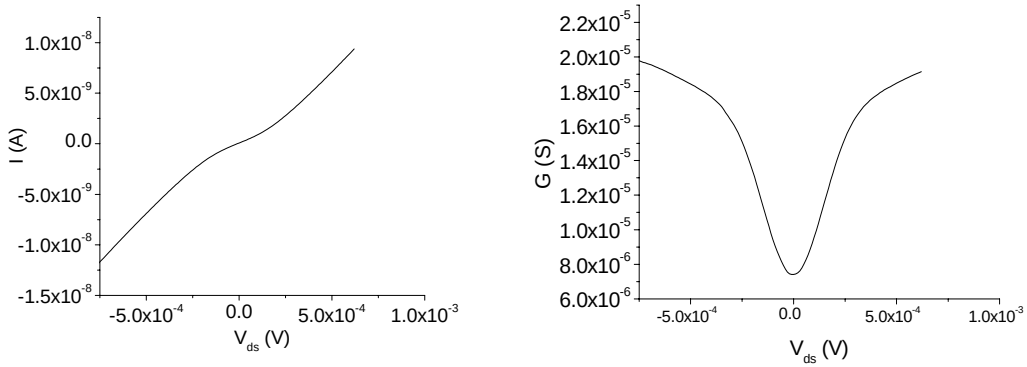


Figure 3.5 The constant calculated (hollow squares) for two junctions at different temperatures from 300 mK to 1.5 K and the low temperature correction of the constant (solid squares).

3.3 Single Electron Charging Effect

3.3.1 I-V Characteristic

When $E_C >> k_BT$, the device is in the blockade region where $-\frac{e}{2C_\Sigma} < V_{ds} < \frac{e}{2C_\Sigma}$. There is no current when the bias voltage is in this region with zero gate voltage applied. On the I-V diagram it shows a flat zone (figure 3.6 (a)). If we consider the differential conductance (*dI/dV*), it shows a dip when the device is in Coulomb blockade region, and a constant conductance when it is out of Coulomb blockade (figure 3.6 (b)).



(a) (b)

Figure 3.6 (a) Current-voltage characteristic of SET. (b) Differential conductance of SET. The I-V measurement is done with zero gate voltage applied.

3.3.2 Coulomb Blockade Oscillations

The SET is DC biased at the peak of the conductance on the G-V_{ds} plot which means the device is in the Coulomb blockade state. By varying the gate voltage,

the number of electrons on the island can be changed one by one and the device can be brought to conducting and blockade states alternately. The V_g dependence of the conductance thus shows periodic peaks as in figure 3.7. The gate capacitance $C_g = e/\Delta V_g \sim 10^{-18}$ F. The finite width of the oscillations is because of thermal excited conducting.

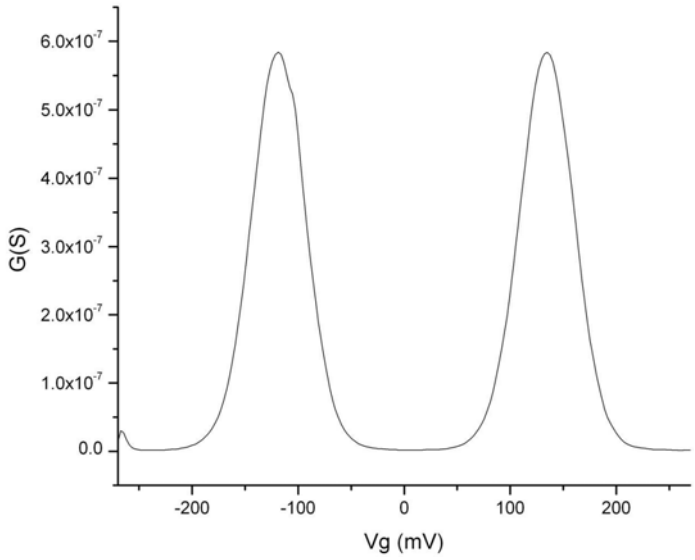


Figure 3.7 Coulomb blockade oscillations. From one peak to the other, the number of electrons on the island is changed by one.

3.3.3 Coulomb Blockade Diagram

Figure 3.8 and figure 3.9 give some examples of Coulomb diagrams as described in chapter 1. On the "Coulomb diamond" graph, the dark diamond regions indicate the blockaded regions where no current flows. The devices are measured at a base temperature of 300 mK where E_C is about 2 to 3 k_BT.

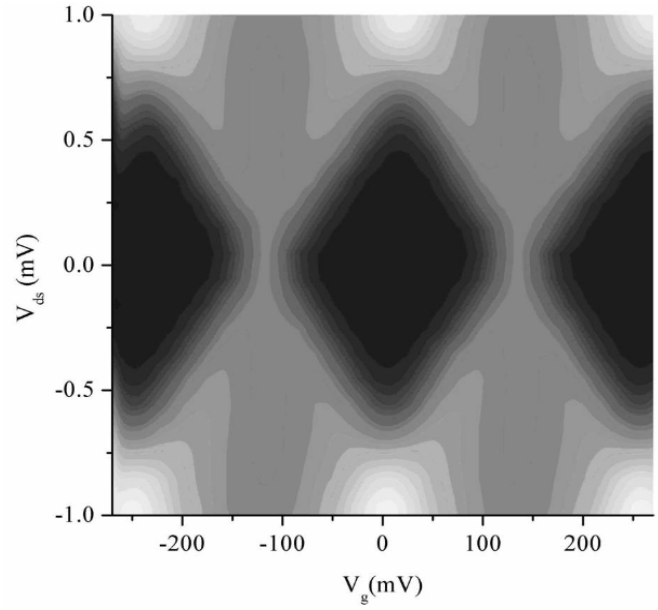
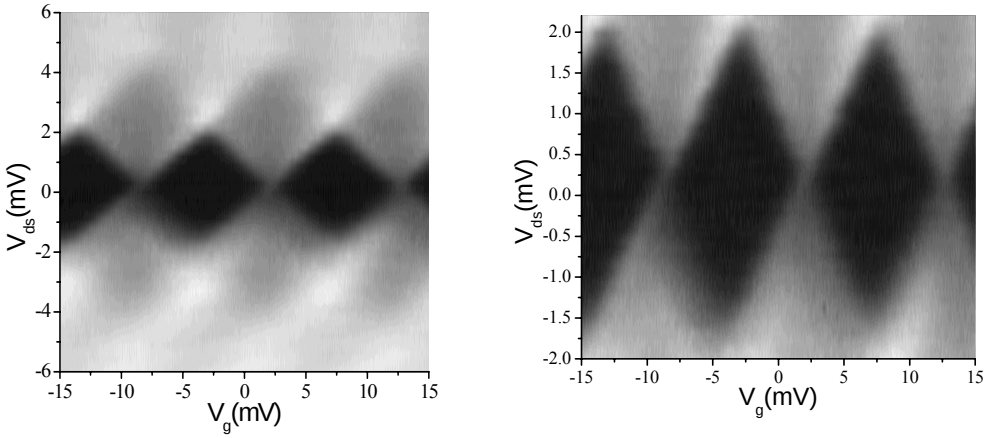


Figure 3.8 Coulomb diagrams of an aluminum SET. In the dark region the conductance is zero, meaning that the current is suppressed. This SET has charging energy of 0.4 meV and the room-temperature resistance is around 700 kOhms.

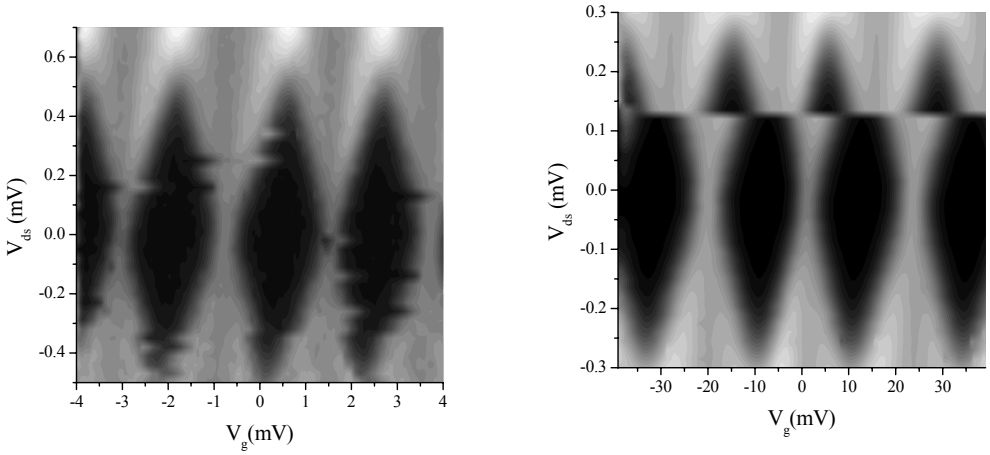


(a)

(b)

Figure 3.9 Coulomb diagrams of an aluminum SET. This SET has a charging energy about 1 meV with a room-temperature resistance around 3 MOhms. (b) Close-up of the central part of (a).

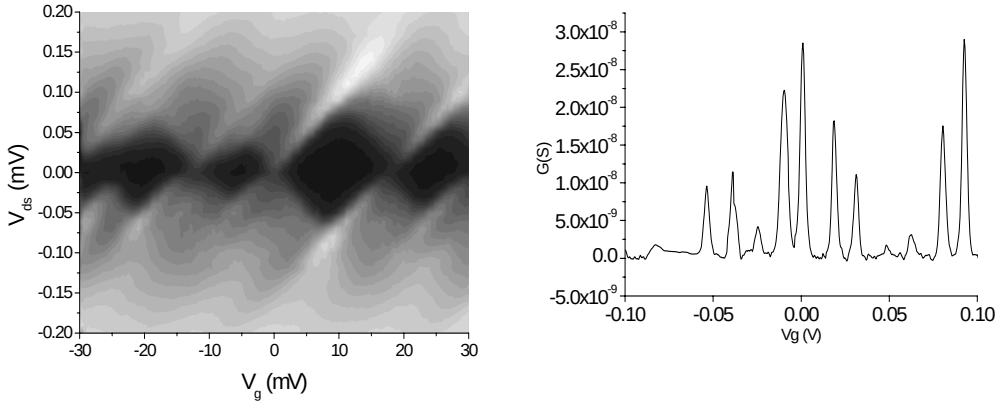
Since an SET is extremely sensitive to the background charge (BGC) change, any ambient charge fluctuation will lead to random shifts in the positions of the peaks of the Coulomb blockade oscillations. The typical stability time for our devices was in the order of tens of minutes, therefore when slow acquisition rate (<10 points /sec) was used to collect the data, BGC causes offsets in the charging diagrams which could be seen in Fig 3.10.



(a) (b)

Figure 3.10 Examples of errors during measurement. (a) The Coulomb diamond shows twisted shape, mostly due to the fluctuation of the background noise. (b) The shift of the shape due to the change of the background charge sensed by the SET.

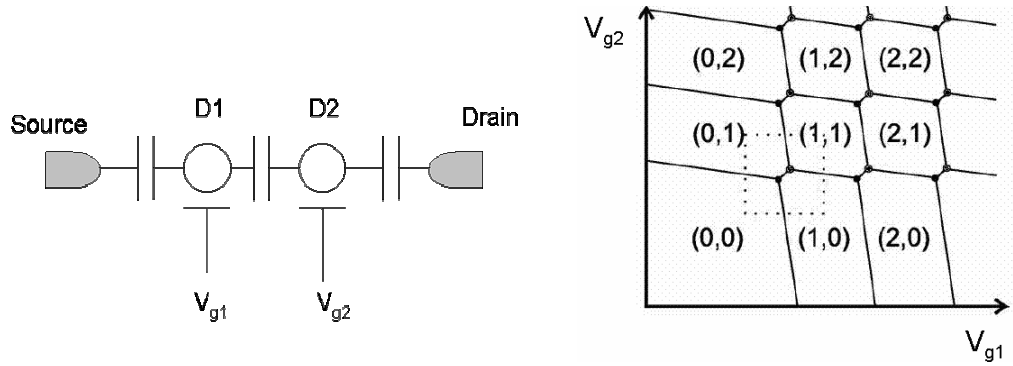
Problems in fabrication also affect the measurement results. Figure 3.11 (a) shows a Coulomb diagram with variable rhombus sizes due to multiple islands. There are probably at least two islands because each oscillation splits into two peaks during the measurements (figure 3.11 (b)) and the spectrum of the oscillations show two different frequencies.



(a) (b)

Figure 3.11 (a) The size of the coulomb diamond varies due to the presence of multiple islands. (b) The peaks of the Coulomb blockade oscillations split into two peaks.

Peak splitting is one of the obvious evidences of transport through a multiple-dot system. The schematic and the charging diagram of a double-dot system are given in figure 3.12. The two solid dots in fig 3.12 (b) show the position of the split peaks. Due to the difference of the gate coupling capacitances in practice, the shape of the charging diagram will be skewed and the height of splitting peaks can be different.



(a) (b)

Figure 3.12 (a) Schematic of a double-dot system. (b) The charging diagram of the system. Dashed line points out the position of splitting peaks [16].

3.4 Radio-Frequency Measurement

The radio-frequency SET measurement is based on reflection and heterodyne detection. By modulating the gate voltage the conductance of the SET can be changed. At the minimum value of the SET conductance, corresponding to the Coulomb blockade state of the transistor, the reflected signal is high. When the SET becomes conducting, some of the signal will be dissipated on the device so the reflected power will decrease. This will cause a change in the reflection coefficient, which is measured by heterodyne detection technique. The reflection coefficient Γ_r is given by:

$$\Gamma_r = \frac{R_{SET} - Z_0}{R_{SET} + Z_0} \tag{3.10}$$

where Z_0 is the characteristic impedance of the coaxial cables in the circuit. Normally the resistance of the SET, R_{SET} is much larger than Z_0 (50 ~ 100 Ω), so that the reflection coefficient is approximated as:

$$\Gamma_r = 1 - \frac{2Z_0}{R_{SET}} \tag{3.11}$$

The modulation of the reflected signal power is given by:

$$D = \frac{P_{R1} - P_{R2}}{P_{R1}} = 1 - \Gamma_r^{\,2} \approx \frac{4Z_0}{R_{SET}} \tag{3.12}$$

where P_{R1} and P_{R2} are the reflected power when the SET is in Coulomb blockade regime and at the peak of the conductance respectively.

Figure 3.13 is the measurement setup. A 3 mm microstrip transmission line (MTL) transforms the impedance of the SET to a smaller value. A bias Tee is used

to isolate the low frequency bias voltage (DC bias plus a small audio-frequency excitation used to monitor the DC source-drain conductance) and the high frequency microwave signal. The low frequency biases are used to monitor the DC source-drain differential conductance from the Lock-in Amplifier. The applied and reflected high frequency signals are separated using a directional coupler. The phase shift of the reflected signal is measured on the oscilloscope by mixing the reflected signal with the applied signal (through a time delay).

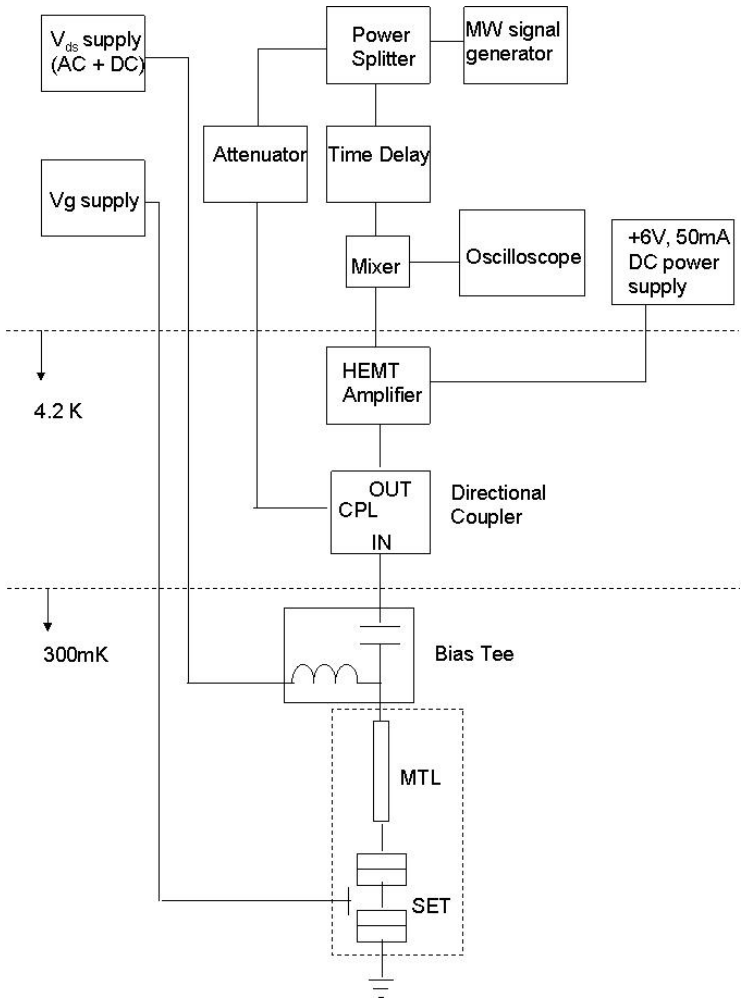
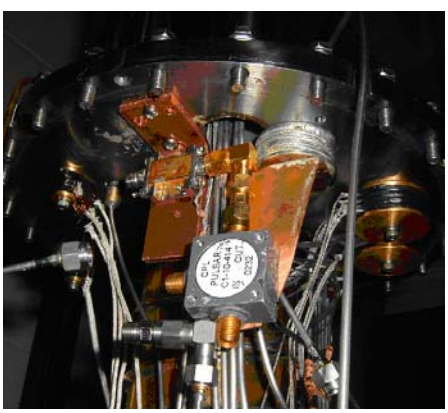
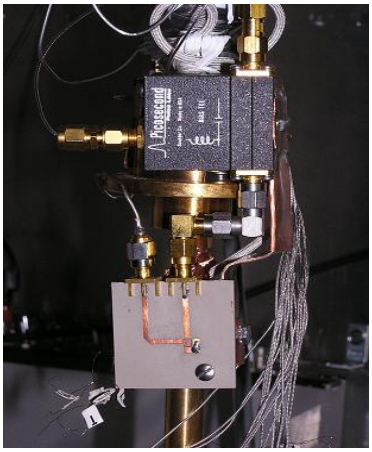


Figure 3.13 Radio-frequency Measurement Setup.



(a)



(b)

(c)

Figure 3.14 (a) Picture of the amplifier and directional coupler thermally anchored to the Inner Vacuum Chamber (IVC) chassis. (b) Bias Tee and the SET microstrip board are thermally anchored to the ^{3}He pot. (c) Structure inside the IVC.

To reduce the heat leakage from the external equipment to the device inside a ^{3}He refrigerator, semi-rigid coaxial cable with Teflon insulator between stainless steel outer shell and center copper conductor is used due to its good thermal insulating and lower parasitic capacitances. The active amplifier is thermally anchored to 4.2 K, and all the cables and other equipments are well anchored, thermally to different temperature stages in the cryostat to reduce the external heating of the device due to power dissipation.

CHAPTER 4

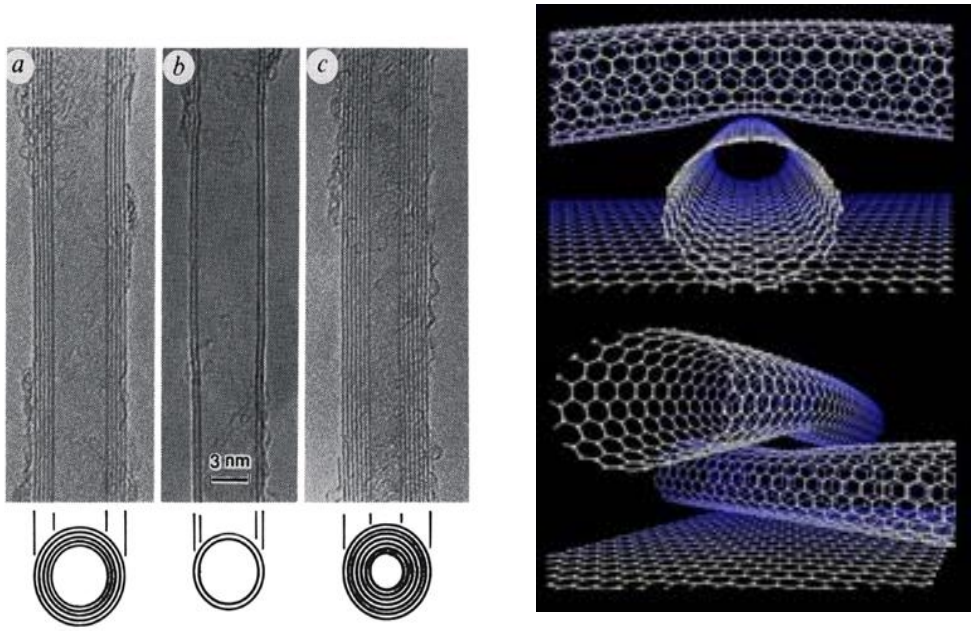
MEASUREMENT OF CARBON NANOTUBE SINGLE ELECTRON TRANSISTORS

4.1 Introduction

Carbon nanotubes (CNT) are fullerene-related structures, but where a C_{60} fullerene molecule is spherical, nanotubes are cylindrical. They are simply graphite sheets wrapped seamlessly onto themselves to form graphite cylinders of a few nanometers in diameter (on the order of one ten-thousandth the width of a human hair) and up to few microns in length. There are two types of carbon nanotubes. One is called single-wall nanotube, or SWNT. This type consists of only one-atom-thick layer of graphite (called graphene), and represents the most promising type for use in transistors. SWNTs often naturally align themselves into a “rope” or “bundled” form where many individual tubes are close-packed in parallel and held together by Van der Waals force. The other type of CNT is multi-wall nanotubes, or MWNTs. They are a group of concentric SWNTs with smaller SWNTs placed inside larger SWNTs.

The multi-wall CNTs were first discovered in 1991 by the electron microscopist Sumio Iijima with the NEC Laboratory in Tsukuba, Japan, who was

studying the material deposited on the cathode during the arc-evaporation synthesis of fullerenes (figure 4.1(a)) [17]. A major event in the development of carbon nanotubes was the formation of single-layer nanotubes in 1993 by S. Iijima, T. Ichihashi and D. S. Bethune *et al* [18] by adding a layer of metals such as cobalt to the graphite electrodes used for arc-evaporation, and by Smalley's group in 1996 using laser-vaporization of graphite [19].



(a) (b)

Figure 4.1 (a) Electron micrographs of microtubules of graphitic carbon. Parallel dark lines correspond to the (002) lattice images of graphite. A cross-section of each tubule is illustrated. *a*, Tube consisting of five graphitic sheets, diameter 6.7 nm. *b*, Two-sheet tube, diameter 5.5 nm. *c*, Seven-sheet tube, diameter 6.5 nm, which has the smallest hollow diameter (2.2 nm) [17].
(b) Schematic of single-wall carbon nanotubes showing that the tubes are sheets of graphene that are rolled up into seamless cylinders [20].

The indexing method developed by Hamada *et al.* for a graphene layer (figure 4.2) determines the convention for describing SWNT nanotubes. When rolling a graphene plane into a cylinder, one of the Bravais lattice vectors $\vec{C} = n\vec{a}_1 + m\vec{a}_2$ of the graphene sheet must satisfy the boundary conditions around the cylinder to fit the whole circumference of the cylinder [21]. $\vec{C}$ is defined as chirality vector, or chiral vector, $\vec{a}_1$, $\vec{a}_2$ are the two primitive lattice vectors and *(n, m)* are a pair of integer indices.

This scheme is very important because it determines the characteristic of individual SWNT nanotube. The *n* and *m* indices can be used to check which of the three categories a nanotube fits in: zigzag, armchair, or chiral [20]. *(n, 0)* type nanotubes are called zigzag nanotubes, and the *(n, n)* types are called armchair nanotubes, otherwise it is called "chiral". Figure 4.3 shows examples of all three.

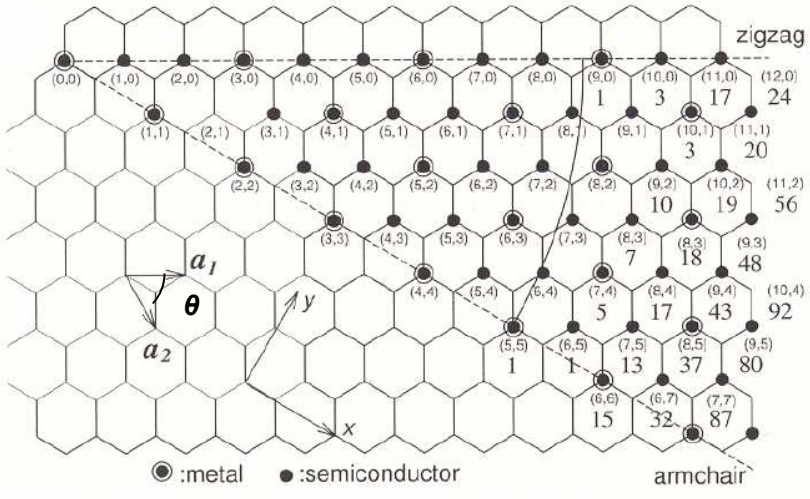


Figure 4.2 Schematic of the indexing method developed by Hamada *et al.* (1992) for single shells of carbon nanotubes. The directions along which lattice points would make armchair and zigzag nanotubes are indicated [21].

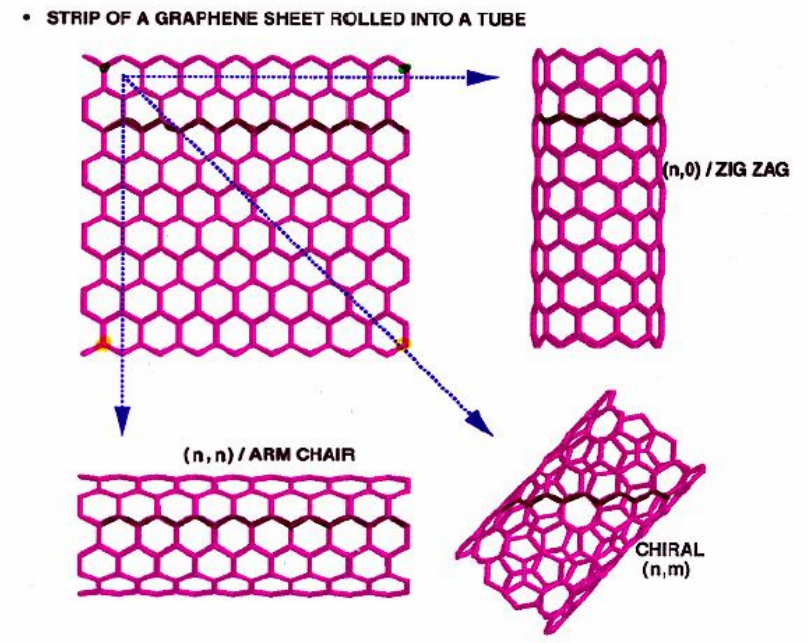


Figure 4.3 Three types of chirality formed by different ways of rolling a graphene sheet: zigzag, armchair and chiral [20].

Another way to describe the chirality vector is to use the chirality angle, θ [21]. The chirality angle is measured between directions of $\vec{a}_1$ and $\vec{a}_2$ as shown in Figure 4.4. It is calculated using this formula:

$$\theta = \sin^{-1} \frac{3m}{2\sqrt{n^2 + m^2 + nm}} \tag{4.1}$$

The electrical properties of carbon nanotubes are quite unique. Unlike most materials, the tubes can either be semiconducting or metallic, the conductivity depending on their diameter and their molecular structure. A simple way to determine if a carbon nanotube is metallic or semiconducting is to look at the indices that describe it. For a given (*n, m*) nanotube, it will be metallic if $n = m$ or $n - m = 3i$, where i is an integer. Otherwise, the tube is semiconducting. Thus the

armchair type nanotubes will always be metallic since $n = m$, while the others can be metallic or semiconducting.

Carbon nanotubes also have unique physical properties such as very good elastic properties, large Young's modulus, and high tensile strength. All nanotubes are expected to be very good thermal conductors along the tube, but good insulators laterally to the tube axis [22]. These qualities make carbon nanotube devices extremely resilient and able to work even in the most inhospitable environment.

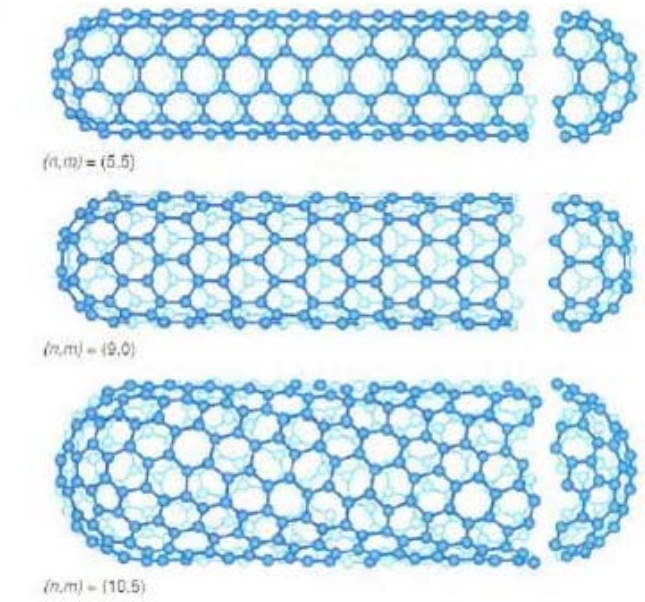


Figure 4.4 Using chirality angle to describe carbon nanotubes: Armchair θ=30º, zigzag θ=0º, chiral 0º<θ<30º [23].

4.2 Fabrication of Carbon Nanotubes

All the SWNT devices measured were fabricated by Motorola Labs using the chemical vapor deposition (CVD) method (figure 4.5). The wafer substrate is patterned with Nickel/Aluminum bilayer catalyst metal (1-5 nm Ni layer on top of 2-10 nm Al layer) before CVD. The nanotubes are selectively grown by having a hydrocarbon gas react with the catalyst. The catalyst islands are defined using electron-beam lithography on the surface of a 2 in. highly doped silicon wafer with 200 nm thermally grown SiO_2. The sample is then placed in the center of the CVD furnace and heated to around 800 degrees Celsius, and methane is used as a precursor gas.

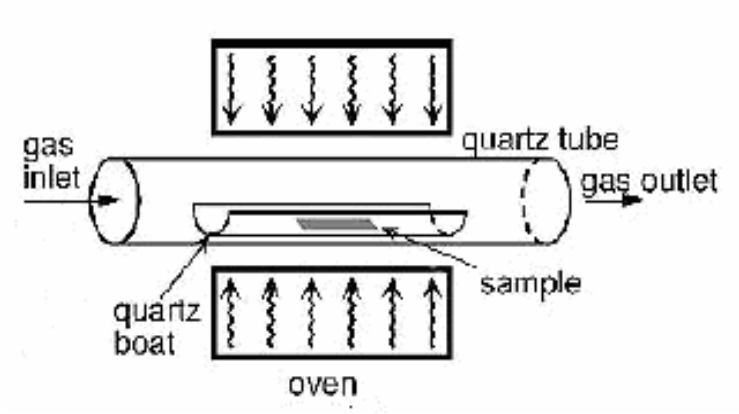
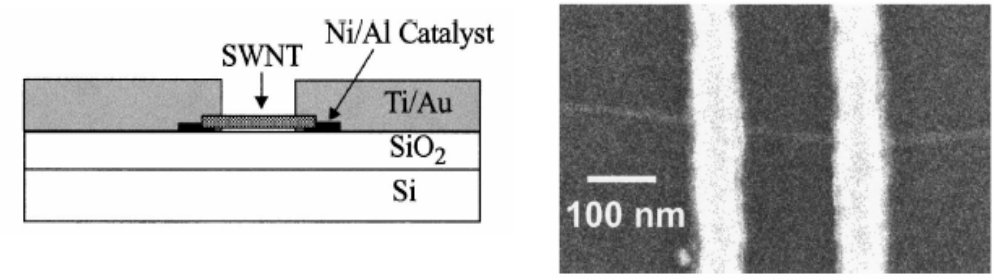


Figure 4.5 Schematic of Chemical Vapor Deposition (CVD). The hydrocarbon gas reacts with the metal catalyst particles on the sample surface to form carbon nanotubes. The temperature of the reaction is normally above 600°C.

The majority of the SWNTs grown by this process have a diameter of 2.7 nm. The effective length of the SWNT is defined by the contacts made to it, which are defined in a subsequent electron-beam lithography step using a liftoff technique. Electrode material consists of 5 nm of Ti and 20 nm of Au. The bottom thin layer

of Ti is used to promote adhesion. A final photolithography step is used to define the bonding pads that consist of 10 nm of Ti and 300 nm of Au. Figure 4.6 shows the schematic of the device structure and an SEM image of a SWNT fabricated by Motorola Labs.



(a) (b)

Figure 4.6 (a) A schematic graph showing the cross-sectional view of the CVD grown nanotube circuit with source and drain leads. (b) A scanning electron microscope image of a pair of metal electrodes bridged by a SWNT. The effective length of the SWNT is defined by the distance between electrodes. [24].

4.3 Carbon Nanotubes as Single Electron Transistors

In carbon nanotube SETs, the nanotube is used as the island of the SET and the island length is defined by the distance between electrodes. The oxidized substrate is used as the gate. The number of the electrons and the energy levels are both quantized. Normally, the tunnel junctions of the SET are formed by the Schottky contacts between the tube and the electrodes [25]. The contact property also determines the large tunneling resistance of the tube (>100 kΩ). The SET must be measured at low temperature because the charging energy is smaller than

room temperature thermal fluctuations. Room temperature operation of nanotube SETs has been achieved by several groups. Postma *et al.* used the tip of an atomic force microscope (AFM) to induce two kinks in a metallic carbon nanotube 25 nm apart [26]. The kinks act as tunnel barriers to electron transport and the total capacitance achievable in this case is about 1 aF. Park *et al.* have used the electrical nicking of a carbon nanotube along its length by an AFM tip to increase the temperature of SET operation [27]. The group of J. B. Cui also achieved room temperature operation of an SET by creating an approximately 10 nm island in a metallic SWNT by local chemical modification using an etch process [29].

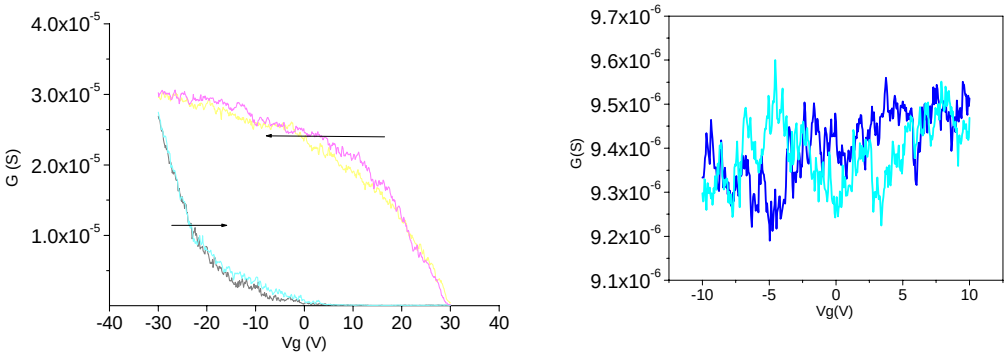
4.4 Measurement of Carbon Nanotube SETs

The same measurement setup as aluminum SETs, which is described in Chapter 2, is used. The measurement of SWNT is done at three temperatures: room temperature, 77 Kelvin and 4.2 Kelvin. The highly doped Silicon substrate is used as a backgate in all measurements. After bonding the devices to a 48-pin chip carrier, the nanotubes are measured first at room temperature to check the conductance between the source and drain electrodes.

The tube type can also be determined by sweeping the gate voltage from negative to positive. The conductance of a semiconducting SWNT normally changes over factor of 10 (Fig. 4.7 (a)). In addition, semiconducting SWNTs mostly exhibit a higher conductance at more negative voltages and the

conductance drops at a positive gate voltage. This shows that the SWNTs are p-type devices. It was also observed that when scanning the gate voltage in different directions the conductance curves form a hysteretic loop; this is mainly due to the charges trapped in the SiO_2 layer which act as an additional backgate voltage.

In a metallic SWNT, the source-drain conductance remains constant, i.e. independent of the applied gate bias. Figure 4.7 (b) shows the conductance of a metallic SWNT at room temperature. As the gate voltage is swept from -10.0 V to +10.0 V, the conductance typically remains around 9.4×10^{-6} Siemens. The fluctuations in the value of the conductance are not repeatable and are likely due to noise in the system.

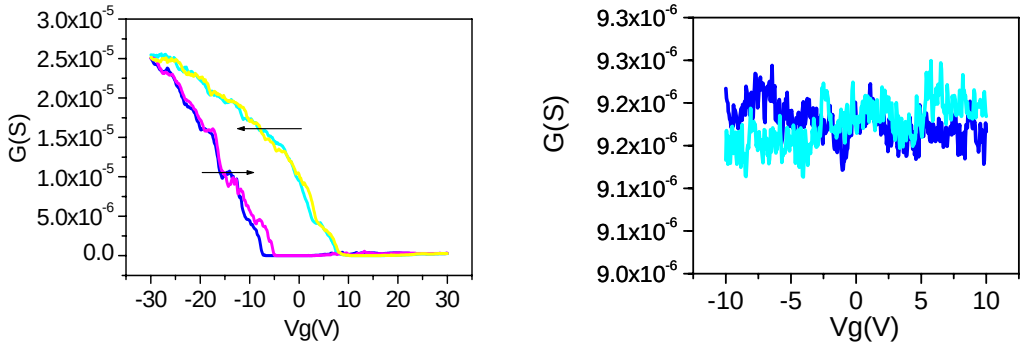


(a) (b)

Figure 4.7 (a) Conductance vs. V_g of a semiconducting CNT at room temperature. It shows strong V_g dependence. The arrows point out the scan direction. (b) Conductance vs. V_g of a metallic CNT at room temperature. The conductance shows no gate voltage dependence.

The devices then are cooled down to 77K, the boiling point of liquid nitrogen, for several reasons. One is to verify the contact between chip carrier and the socket where the chip carrier sits. The other is to check the low temperature behavior of the CNTs. It was noticed that some of the semiconducting CNTs were frozen out at this temperature, showing no conductance at any gate voltages. From Fig. 4.8 (a) it can be seen that the hysteretic loop of the conductance almost disappears at low temperature possibly due to the freeze-out of the highly doped substrate. And it has much less fluctuation than at room temperature (Figure 4.8 (b)).

One of the devices shows ambipolar behavior (figure 4.9). It shows p-type behavior in the negative gate voltage region and n-type behavior in the positive gate voltage region with an insulating region in between. The ambipolar behavior is due to the large diameter (>3 nm) of the semiconducting SWNT since the larger diameter the smaller the bandgap of semiconducting SWNT. It is easier for the Fermi level to reach the conduction band at higher positive gate voltage.



(a) (b)

Figure 4.8 Conductance vs. Vg at 77K of (a) a semiconducting CNT and (b) a metallic CNT.

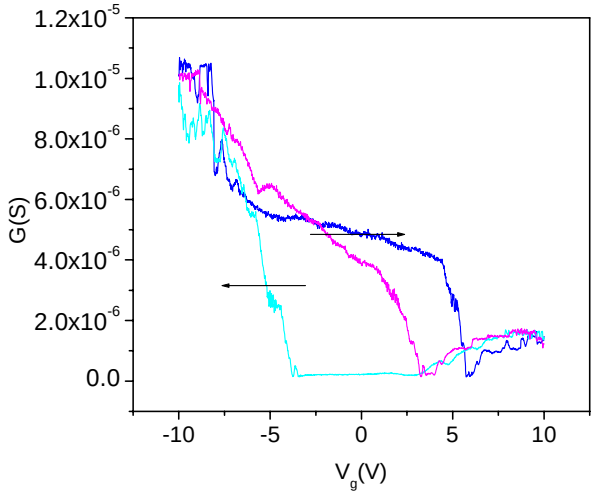


Figure 4.9 One of the devices shows ambipolar behavior at 77K. It shows p-type behavior at negative gate bias and n-type behavior when positive bias larger than 3 volts. The conductance is lower in n-region than in p-region.

The final step of the measurement is done at 4.2K, the boiling point of liquid helium. At this temperature it is possible for us to observe single charging effects because the charging energy now can be greater than the thermal energy.

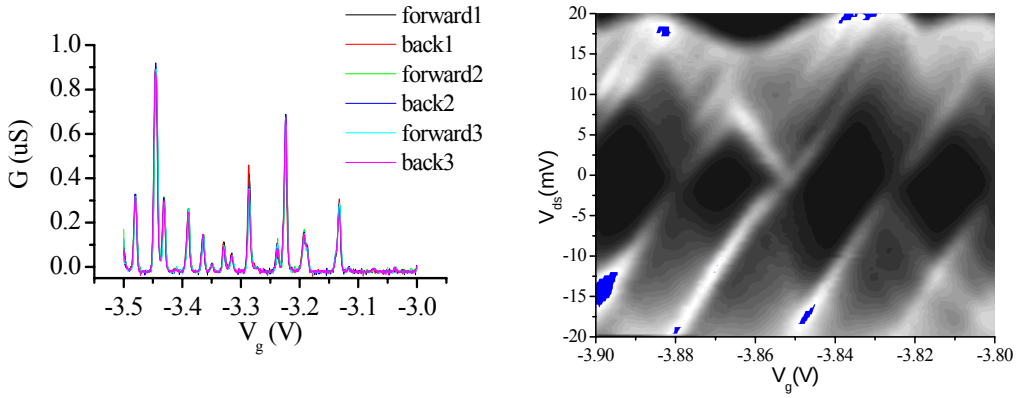
Several semiconducting SWNTs showed Coulomb blockade oscillations (Figure 4.10 (a)) and charging diagrams are also measured in these devices. The conductance at the peak of the oscillations is normally below 1 MOhms, and the peak-valley ratio is greater than 10. From figure 4.10 (a) it can be seen that the hysteresis caused by the different V_g scan direction has totally disappeared. The black regions in figure 4.10 (b) represent the Coulomb blockade of zero current. All these prove that the transistor behaves as an SET. The charging energy of this device shown in figure 4.10 (b) is approximately 5 meV, which is typical for

semiconducting SWNTs. The approximate gate coupling capacitance can be obtained from the period of the oscillations since $C_g=e/\Delta V_g$. For this device C_g is about 10^{-17} Farad. The junction capacitances C_j can be calculated using the charging energy $E_C = \frac{e^2}{2C_\Sigma} = \frac{e^2}{2(2C_j + C_g)}$ to be ~ 10^{-18} Farad. Therefore we can conclude that $C_g > C_j$ and the charging energy is dominated by C_g. It is quite possible to achieve a voltage gain greater than unity out of SWNT SETs since [10]:

$$K_V = \frac{V_{ds}}{V_g} = \frac{C_g}{C_1} \tag{4.2}$$

C_1 is the capacitance of the first tunnel junction. For the device in figure 4.10, the K_V is about 10.

All these characteristics make SWNT suitable for the radio frequency (RF) measurement which is our next goal.



(a) (b)

Figure 4.10 Single electron effects measured at 4K. (a) Coulomb oscillations shown by one of the semiconducting SWNTs. (b) Coulomb diamonds of this device.

Figure 4.11 shows the Coulomb oscillations at different temperatures of the same device exhibiting oscillations up to 50 K. This also indicates the charging energy of this carbon nanotube SET is around 5 meV.

With lowering the temperature, the width of oscillations becomes narrower and the peak becomes higher. This also indicated resonant tunneling effect.

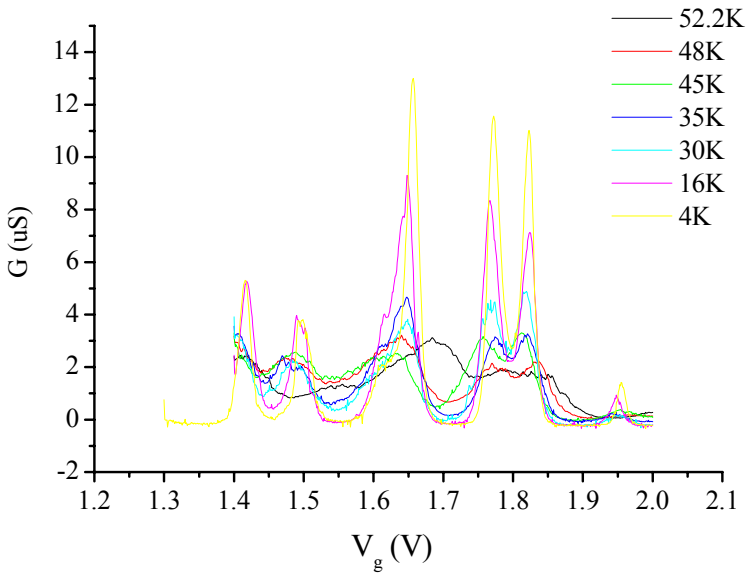


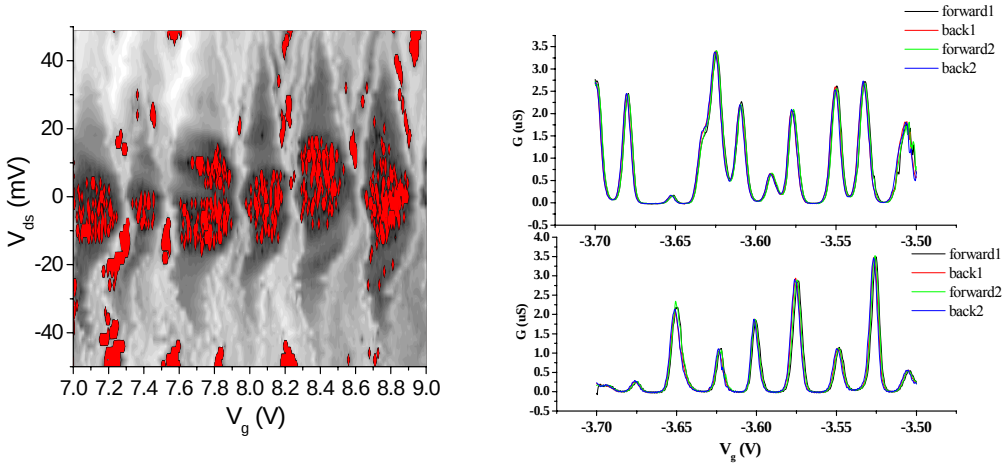
Figure 4.11 Temperature dependence of Coulomb oscillations.

4.5 Problems in Measurements

Several problems are encountered during the measurements. Figure 4.12 (a) shows a twisted Coulomb diagram. The twisting might due to the fluctuation of the background charge during each V_g scan, or the shift of the conductance peaks for each scan caused by hysteresis.

Figure 4.12 (b) shows a major problem with stability in the measurements of

carbon nanotubes. These two curves were measured under the same condition in two consecutive days and the peaks of the oscillations appeared at different places although the oscillations were all quite repeatable over the period of data acquisition. Figure 4.13 has the same problem. These two diagrams are from two sequential measurements in the same ambient condition with same biases and measurement technique, but two different charging diagrams are observed.

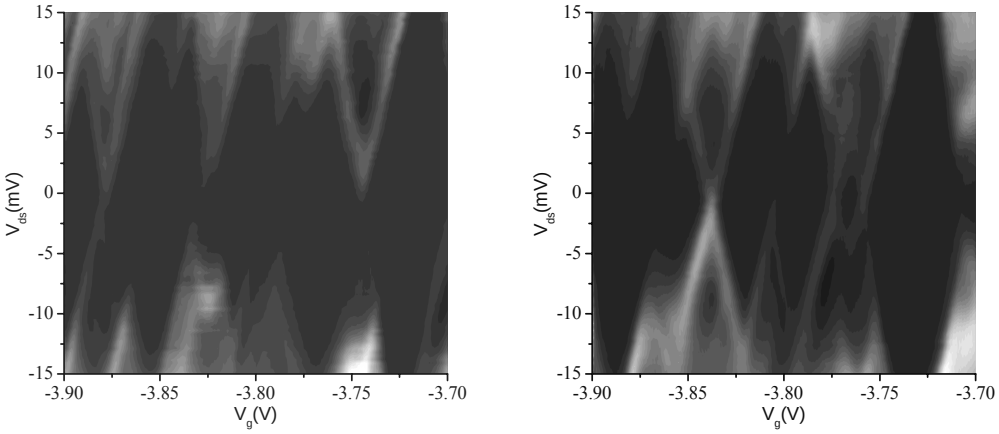


(a) (b)

Figure 4.12 (a) A twisted charging diagram shown by one of the SWNTs. (b) Coulomb oscillations measured in the same Vg range in two sequential days. Although there was no hysteresis in both measurements, it showed substantially different oscillation signatures.

During the measurement the devices showed good short-term stability but the long-term stability is poor. This instability is mostly due to the interference of the background charges, mostly in the silicon dioxide layer or introduced by potential fluctuations on nearby nanotubes. To date, there has not been a good way to

suppress this effect.



(a) (b)

Figure 4.13 Two sequential measurements at the same region of V_g and V_{ds} but showing different charging diagrams due to the effect of background charge.

CHAPTER 5

SUMMARY AND FUTURE WORK

5.1 Summary

Aluminum single electron transistors have been successfully fabricated and Coulomb blockade effects are observed. During the fabrication it has been found that the tunneling resistance can be roughly controlled by the time and pressure of the *in-situ* oxidation. It also has been demonstrated that in the higher temperature region where coulomb blockade is weak, the SETs show primary thermometer and secondary thermometer behaviors.

Carbon nanotubes also show single electron charging effects at low temperature, which means carbon nanotubes can be used as SETs. The Coulomb oscillations and Coulomb blockade are clearly demonstrated. The charging energy of carbon nanotube SETs are normally higher than aluminum SETs, so it is possible to make carbon nanotube SETs operating at much higher temperatures.

5.2 Problems

Background charge fluctuations are the major problem encountered during measurements. It is also believed to be the main source of 1/f noise and if the

accumulated charge is large enough it can shift the Coulomb blockade [28] just as seen in carbon nanotube SET measurements. There are many sources of charge offset. Besides the obvious ones such as nearby electrodes, an importance source is the traps or defects in the SiO_2 substrate layer or at the interfaces between substrate and devices. In principle there also might be defects such as pin holes inside the AlO_x tunneling barriers, but since the barrier size is extremely small, the possibility of encountering a defect is very low.

5.3 Future Work

5.3.1 Control of Tunneling Barrier

In Chapter 3 one way to control the thickness of tunneling barriers is demonstrated. Another possible way is to change the oxidation time of the *in-situ* oxidation with a fixed pressure instead of varying the pressure. This might give a better quality oxide layer due to the higher density of oxygen available.

Furthermore, plasma-grown AlO_x might be preferable to thermally-grown AlO_x due to its higher density and uniformity. These effects will be explored in future work.

5.3.2 RF-SET

The RF-SET is one of the fastest, ultra sensitive electrometers available. The

failure of previous experiments is due to the high resistances of the Al SET devices (~1 MΩ), thus the modulation of the signal is too small to detect. Since obtaining low resistance devices (~100 kΩ) is quite possible due to the improved oxidation control, the RF measurement should be possible for Al SETs.

RF measurements of CNT-SETs are also promising. CNT-SETs normally show suitable resistance of a few kilo-Ohms and the charging energy is quite high (≥4 meV), it has charge sensitivity equal to or higher than Al-SET, all these characteristics make it a good option for RF measurements.

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